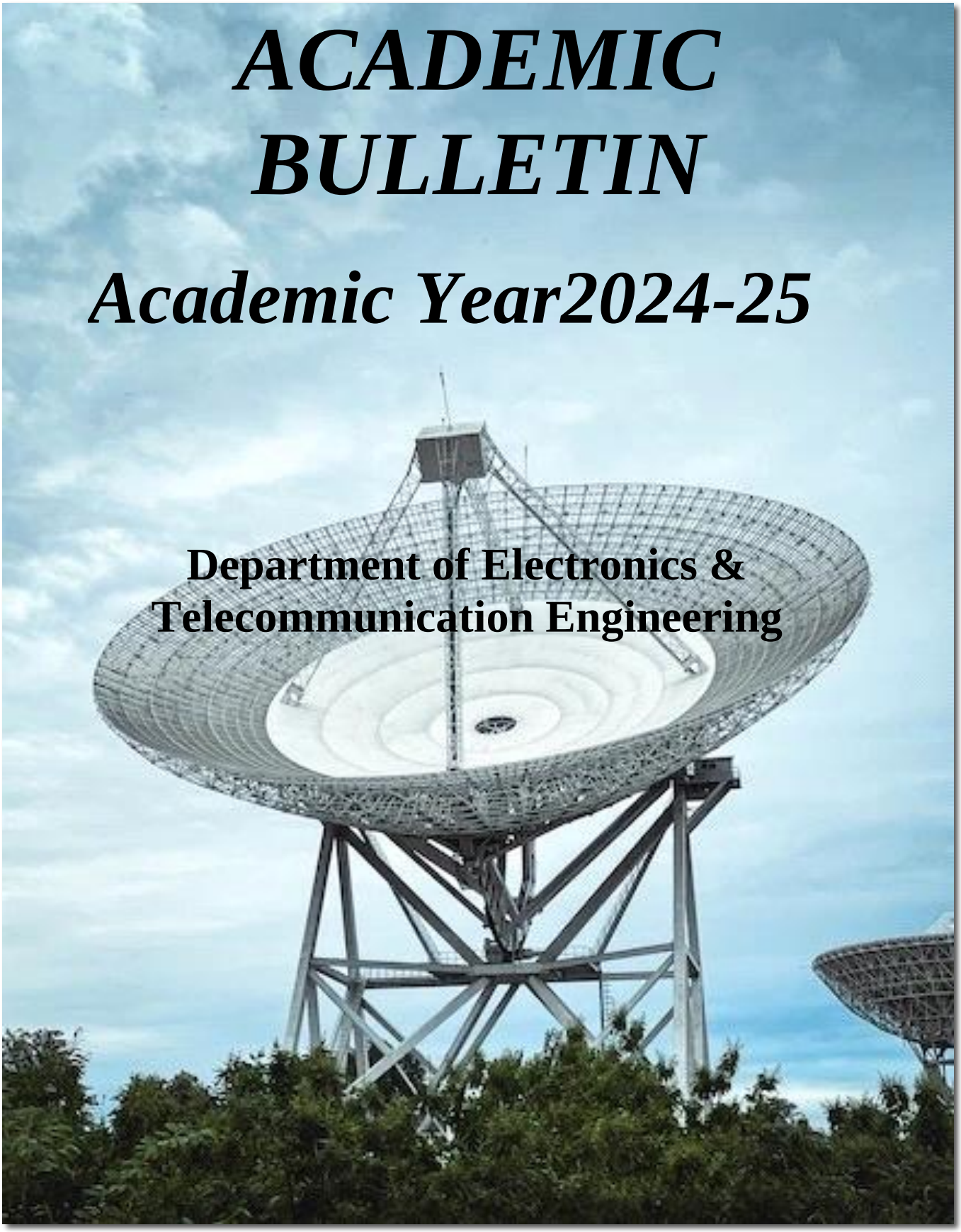
Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

ACADEMIC BULLETIN

Academic Year2024-25



Department of Electronics & Telecommunication Engineering

Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

ACADEMIC BULLETIN

July 2024- December 2024

Department of Electronics & Telecommunication Engineering

Prepared by:

Prof. Supriya Dicholkar
(Assistant Professor, EXTC, DJSCE)

Prof. Amit A. Deshmukh
(Professor & Head EXTC, DJSCE)

ACADEMIC BULLETIN

Period: 1st July 2024 – 31st December 2024

Department of Electronics and Telecommunication

1. ABOUT DEPARTMENT

1.1 Department Information

- Started in the year 1999 with the intake of 30 and which was increased to 60 in the subsequentyear.
- The intake was increased to 120 in the Academic Year 2010 – 11.
- In the Academic Year 2011 – 12, Department has started M.E. Program in Electronics & telecommunication with an intake of 18 students.
- For the first time Department got NBA accreditation for two years from January 2013. In second Outcome based evaluation, Department got NBA accreditation for three years from July 2017.
- The Department started with Ph.D. program in Academic Year 2015 – 16 with an intake of 10 students.
- The department is having highly qualified, experienced and dedicated faculties and supportingstaff.
- Well-equipped labs and fully air-conditioned classrooms with projectors.
- The intake was increased to 180 in the Academic Year 2022 – 23.

1.2 Vision of the Department

To develop technically competent and socially responsible Electronics and Telecommunication engineers capable of fulfilling expectations at indigenous and global levels.

1.3 Mission of the Department

- To provide a conducive educational environment for students by providing goodinfrastructural facilities, knowledge base and excellent faculty support.
- To provide a strong foundation of core knowledge and exposure to research culture.
- To motivate learners to acquire adequate professional and soft skills, to develop personalitytraits and eventually transform them as life-long learners.
- To strive and achieve practical exposure by maintaining good rapport with industry and professional network.

1.4 Program Educational Objectives (PEOs)

- **PEO1: To prepare learners for graduate studies by providing strong foundation of basic sciences,computer programing and thus, develop analytical aptitude, and problem-solving abilities.**
- **PEO2:** To develop a fundamental understanding of electronic & integrated circuits, communication systems and allied disciplines.
- **PEO3:** To develop core competency and expertise in the diverse areas of communication covering Signal processing, Electromagnetic Engineering, Embedded Systems, ComputerCommunication and Advanced Wireless Networks domains.
- **PEO4:** To inculcate competencies and aptitude in extending acquired technical knowledge to solve real life issues with high professional and ethical standards.
- **PEO5:** To develop proficiency in soft skills and deliver adequate personality traits to enablethe pass outs to pursue higher education, to find competitive employment opportunities and/or pursue entrepreneurial ventures.

1.5 Program Specific Outcomes (PSOs)

- Design and implement electronic systems that perform analog and digital signal processing functions as applied in embedded systems, multimedia processing and VLSI design.
- Design and implement necessary components (circuits, antennas, microwave devices) of modern RF/Wired/Wireless communication systems.
- Cultivate necessary soft skills, aptitude and programming skills to solve real-world problems.

2. ADMINISTRATION

IETE COMMITTEE

Prof. Amit Deshmukh — Dr. Anuja Odhekar

PROJECT COORDINATOR

Prof. Amit Deshmukh — Dr. Ameya Kadam

DEPARTMENTAL LIBRARY

Prof. Amit Deshmukh — Prof. Archana Chaudhari

ALUMNI COMMITTEE

Prof. Amit Deshmukh — Prof. Ranjushree Pal

NBA CORE COMMITTEE

Prof. Amit Deshmukh — Dr. V. V. Kelkar (PC/NC)

Dr. Ameya Kadam — Dr. Venkata A. P. Chavali

AUTONOMY COMMITTEE

Dr. S. B. Deshmukh — Dr. Poonam Kadam

TIME-TABLE COMMITTEE

Dr. Venkata APC — Prof. Archana Chaudhary

PLACEMENT COORDINATOR

Dr. Aarti Ambekar

NPTEL and IBM COORDINATOR

Dr. V. V. Kelkar

Department of Electronics and Telecommunication

3. IETE- SF

The Electronics and Telecommunication Department of Dwarkadas. J. Sanghvi College of Engineering presents Institution of Electronics and Telecommunication Engineers- Student Forum (**IETE-SF**). The student chapter with a working force committee of 22, consisting of **second year** and third **year students**, hosted a few of the most quintessential and technically challenging events. A membership drive was conducted at the start of the year with an overwhelming response. (www.djsceietesf.com)

IETE Organizing Committee Structure

IETE SF Branch Counsellor: - Dr. Anuja Odhekar

Chairman	Utkarsh Lotiya
Vice-Chairperson (Admin)	Aneesh Joshi
Vice-Chairperson (Technical)	Samay Mehta
Secretary	Radhika Kadu
Treasurer	Gauransh Singh Bedi
DJ-Strike Co-ordinator	Harshil Khara Vaishnavi Pawar Manjiri Kale Shravanee Madhale

Head Of Departments:	
Publicity	Isha Solanki Vinil Shah
Marketing	Purav Ashar Nandini Mandekar
Technical	Sairudra Gudur
Infotech	Prashant Sherkar
Creatives	Nidhi Gandhi Parth Mehta
Events	Aditya Naik
Book Bank	Kartik Panchal
Component Bank	Kartik Panchal

3. DEPARTMENT ACTIVITIES

3.1 Value Added Program under IETE-SF

Book Bank

IETE-SF provides the students with a book bank facility where they can issue reference books at nominal rates for the entire semester. Students who want a better insight into the subject avail this facility as these reference books aid in developing a good understanding of the topics and enable them to consolidate their foundation of the subject. Book bank has more than 60 book titles as per the syllabus requirement for 3rd to 8th semester. This activity not only motivates students to use reference books prescribed in syllabus but also explore them in the library management system. The alumni who worked as "Book-Bank" coordinators received paid assistance-ship in the library during their master program.

Component Bank

IETE-SF provides a component bank facility where students can borrow electronic components which they require for executing multiple projects both in and outside of the curriculum. They can utilize the facility by initially paying 50% of the cost and getting a refund of 20% on returning the components, provided that they are undamaged.

Department of Electronics and Telecommunication

3.2 Workshop on MATLAB Programming under IETE-SF

Speakers: Dr. Satish Chavan, Dr. Sunil Karamchandani, and Prof. Ranjushree Pal,

Association of the Speakers Associate Professor, EXTC, DJSCE, Mumbai

Date of the Session: 20th to 23th of August 2024

No. of Participants: 94

Participants: SE and TE Students

Objectives of the activity:

- To make the students familiar with a new software.
- To make use of the MATLAB Programming commands to problems in different mathematical subjects.

Contents:

The age-old tradition of the MATLAB workshop conducted by IETE-ISF saw an overwhelming response this year. Conducted from August 20 to 23, 2024; it was a comprehensive four-day event designed to enhance participants' skills in MATLAB. The workshop offered a structured progression from fundamental concepts to advanced applications, ensuring that attendees developed a strong grasp of the software. Led by experienced instructors, including Dr. Satish Chavan, Dr. Sunil Karamchandani, and Prof. Ranjushree Pal, the workshop covered key areas such as MATLAB basics, image processing, data analytics, and data visualization. Each session was hands-on, allowing participants to apply what they learned in real-time, thus reinforcing their understanding and proficiency. This report summarizes the workshop's content and outcomes, highlighting the essential skills gained by participants, which are crucial for solving complex problems using MATLAB in various professional and academic settings. The participants received certificates after attending all four days.

Day 1: August 20, 2024

On the first day of the MATLAB Workshop, participants established a foundational understanding of MATLAB. This session covered the essentials of MATLAB, from understanding its environment to mastering basic operations. Led by Dr. Satish Chavan, participants gained a solid grounding in the core concepts of MATLAB that served as the building blocks for more advanced topics in the coming days.

Topics Covered by Dr. Satish Chavan:

Basics of MATLAB: Introduction to MATLAB, Overview of MATLAB's interface, Basic commands and syntax, Variables and data types, Control structures (loops, conditionals).

MATLAB Environment: Navigating the MATLAB desktop environment, Customizing the layout and preferences, Introduction to MATLAB Editor, Command Window, and Workspace.

Matrices and Operators: Matrix creation and manipulation, Basic matrix operations (addition, subtraction, multiplication), Element-wise operations, Special matrices (identity, zeros, ones), Matrix indexing and slicing.

Functions in MATLAB: Writing and using functions, Function syntax and structure, Input and output arguments, Scope and variable visibility, Built-in functions and libraries.

Day 2: August 21, 2024

On the second day of the MATLAB Workshop, participants focused on the practical applications of MATLAB in image processing. Led by Sunil Sir, this session explored the powerful Image Processing Toolbox. Image processing is essential in fields such as computer vision, medical imaging, and multimedia. Attendees learned how to apply

MATLAB's extensive tools to perform complex image analysis tasks. The day included hands-on exercises to help participants understand image data handling, processing techniques, and practical applications.

Topics Covered by Dr Sunil Karamchandani:

Image Processing Toolbox: Introduction to the Image Processing Toolbox, Image data types and formats, Basic image processing operations (filtering, transformations), Image enhancement techniques, Object detection and segmentation, Practical examples and applications.

Day 3: August 22, 2024

On the third day, the workshop focused on Data Analytics using MATLAB. This session was led by Prof Ranjushree Pal who guided us through various aspects of data analysis, from representation to prediction. Participants learned essential techniques for analyzing and representation of data, as well as exploring statistical data, to turn insights into actionable outcomes.

Topics covered by Prof Ranjushree Pal:

Data Representation: Types of data structures (tables, arrays, cell arrays), Importing and exporting data, Data cleaning and pre-processing.

Basic Statistical Data Analysis: Descriptive statistics (mean, median, mode), Measures of dispersion (variance, standard deviation), Correlation and covariance.

Statistical Hypothesis Testing: Understanding hypothesis testing concepts, T-tests and ANOVA, Chi-square tests, p-values and significance levels.

Day 4: August 23, 2024

The final day of the workshop was continued by Prof Ranjushree Pal. She guided the participants through the final stages of data visualization and analysis in MATLAB. Students were able to visualize data and use EDA to identify patterns and anomalies. Additionally, a brief introduction to machine learning and predictive modelling was given.

Topics covered by Prof Ranjushree Pal:

Data Visualization: Creating plots and graphs (line plots, bar charts, histograms); customizing visualizations (labels, legends, colours); and advanced visualization techniques (3D plots, heat-maps).

Exploratory Data Analysis (EDA): Techniques for EDA, Identifying patterns and anomalies, Summary statistics and graphical representations.

Data Prediction: Introduction to predictive modelling, Regression analysis (linear and nonlinear), Model evaluation and validation, Introduction to machine learning concepts in MATLAB.

Conclusion:

The MATLAB Workshop held from August 20 to 23, 2024, at Dwarkadas J Sanghvi College of Engineering, provided participants with a comprehensive introduction to MATLAB, progressing from foundational concepts to advanced applications. Across the four days, participants gained essential skills in MATLAB's environment, explored image processing techniques, and delved into data analytics. The workshop concluded with an in-depth focus on data visualization, exploratory data analysis (EDA), and an introduction to predictive modeling and machine learning. This structured approach, guided by experts like Dr. Satish Chavan, Dr. Sunil Karamchandani, and Prof. Ranjushree Pal, equipped attendees with practical knowledge and hands-on experience, making

them proficient in using MATLAB for a wide range of applications. The workshop not only strengthened the participants' technical abilities but also prepared them to tackle complex real-world problems using MATLAB.

Photographs of the Event:





3.3 Seminar on VLSI Design Flow & Integration with FPGA

Faculty Members: Prof. Poonam Kadam
Date of the session: 1st October 2024
No. of Participants: 30

Participants: SE students, TE students & Faculty members of EXTC department.

Contents:
The seminar on "VLSI Design Flow & Integration with FPGA" provided a comprehensive overview of the intricate process of designing and implementing Very-Large-Scale Integration (VLSI) circuits, with a particular focus on the role of Field-Programmable Gate Arrays (FPGAs) in the design process. Prof. Poonam Kadam, a distinguished expert in the field, delivered an enlightening presentation that captivated the audience.

Key Takeaways:

- **VLSI Design Fundamentals:** The seminar began by introducing the fundamental concepts of VLSI design, including the various stages involved in creating integrated circuits.
- **FPGA as a Prototyping Tool:** Prof. Kadam highlighted the significance of FPGAs as a rapid prototyping tool in VLSI design. FPGAs offer a flexible and efficient platform for testing and verifying designs before committing them to silicon.
- **Design Flow Stages:** The presentation delved into the specific stages of the VLSI design flow, from specification and logic design to synthesis and physical implementation.
- **Hands-on Demonstration:** To reinforce the theoretical concepts, a live demonstration was conducted, showcasing the practical aspects of designing and implementing a circuit using FPGA.
- **Challenges and Solutions:** The speaker addressed the common challenges faced in VLSI design, such as power consumption, timing constraints, and design complexity. Effective strategies to overcome these challenges were discussed.
- **Future Trends:** The seminar concluded with a glimpse into the future of VLSI and FPGA. Prof. Kadam emphasized the growing importance of these technologies in emerging fields like AI, 5G, and IoT.

Conclusion

The seminar on "VLSI Design Flow & Integration with FPGA" was a valuable learning experience for the attendees. Prof. Poonam Kadam's expertise and engaging presentation provided a clear understanding of the complex world of VLSI design and the pivotal role of FPGAs in the development of modern electronic systems. The seminar not only enriched the participants' knowledge but also inspired them to explore the exciting possibilities offered by these technologies.

Event Pictures:

3.4 Seminar on 'Role of Engineers in Armed Forces'

Guest Speaker: Tanaya Parab, Distinguished Alumna of DJSCE
Date of the session: 23rd September 2024
No. of Participants: 100

Participants: SE students, TE students & Faculty members of EXTC department.

Introduction

On 23rd September 2024, the IETE-ISF of Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized a seminar titled "The Role of Engineers in Armed Forces." The session featured Tanaya Parab, an esteemed alumna, who shared her journey from engineering student to serving in the defense forces. The seminar aimed to inspire students to explore careers in the armed forces and understand the critical role of engineers in defense.

Key Points from the Seminar

Distinguished speaker, Tanaya Parab's presentation was highly engaging and structured around the following key themes:

1) College Life and Early Passion for the Armed Forces:

The speaker began by sharing her personal experience at DJSCE, explaining how her college days ignited her interest in the armed forces. She spoke about her initial motivation, curiosity about defense careers, and how she balanced her academic achievements while paving the way toward her passion. Her journey demonstrated that determination and a clear focus from an early stage can lead to remarkable careers.

2) Need for Greater Exposure to Armed Forces in Urban Institutions:

A key theme was the lack of awareness about defense career opportunities in urban areas and elite educational institutions. The speaker urged colleges and student forums like IETE-ISF to organize more such initiatives to bridge this gap, stating that many students in urban settings often overlook the armed forces, despite its offering some of the most fulfilling and challenging roles for engineers.

3) Entry Pathways into the Army, Navy, and Air Force:

The speaker provided an in-depth overview of the various entry schemes available for engineers to join the armed forces, such as the Technical Graduate Course (TGC), University Entry Scheme (UES), and Air Force Common Admission Test (AFCAT). She explained the selection criteria, age limits, and technical qualifications for each pathway, offering clarity on how students can pursue careers in the defense sector.

4) Understanding Permanent vs. Short Service Commission:

The seminar also covered the distinctions between Permanent Commission (PC) and Short Service Commission (SSC) in the armed forces. The speaker illustrated the benefits of each, noting that while PC offers a long-term career in the forces, SSC provides a platform for those seeking to experience defense life for a limited period while still making significant contributions.

5) Services Selection Board (SSB) Process:

A major highlight was the detailed explanation of the SSB (Services Selection Board) process. The speaker walked the audience through each stage of the process, from initial screening and psychological evaluations to group tasks and personal interviews. She shared personal tips for success, such as

focusing on Officer-Like Qualities (OLQs) and remaining authentic during interviews, while encouraging students to view setbacks as learning opportunities.

6) Role of Engineers in Technical Regiments:
The speaker elaborated on the roles engineers play in various technical regiments within the Army, stressing that engineers are crucial in maintaining, designing, and upgrading defense technologies. She emphasized that disciplines like electronics, telecommunications, mechanical engineering, and computer science are vital to the modernization and operational success of the defense sector.

7) Engineers as Innovators in Defense Technology:
Highlighting the growing role of technology in modern warfare, the speaker described engineers as the backbone of the military's technological edge. She emphasized their contributions to developing advanced communication systems, AI in defense, and other cutting-edge technologies, reinforcing the importance of engineering expertise in maintaining national security.

8) Advantages of a Career in the Armed Forces:
The speaker spoke passionately about the numerous benefits of joining the armed forces, including leadership development, personal growth, adventure, and job security. She explained that the defense forces offer unique opportunities to serve the nation with honor, stating, "In the forces, every day is an opportunity to grow as a leader and serve with purpose. It's more than a career—it's a way of life."

9) Comparison Between Armed Forces and Civilian Life/Foreign Education:
The speaker compared the structured, disciplined lifestyle of the armed forces to the often unstructured and high-stress environment of corporate jobs and foreign education. She highlighted the camaraderie, sense of purpose, and pride that comes with serving in the defense forces—qualities that are often difficult to find in civilian life.

10) Glimpse into Her SSB Journey:
Drawing from her personal experience, the speaker shared stories of the emotional highs and lows of her SSB journey—the challenges she faced, the lessons she learned, and the joy of finally being selected. Her anecdotes provided a realistic and motivating look into the selection process, offering students a tangible sense of what it takes to succeed.

11) Developing Officer-Like Qualities (OLQs):
In the final segment, the speaker focused on the importance of developing Officer-Like Qualities (OLQs), such as leadership, teamwork, resilience, and communication. She advised students to cultivate these qualities through active participation in college activities, sports, and self-reflection, offering practical tips for personal growth.

Interactive Q&A

The seminar concluded with a lively Q&A session, where students sought advice on topics like SSB preparation, developing leadership skills, and balancing technical innovation with military traditions. The speaker's responses were insightful and practical, further engaging the audience.

Conclusion

The seminar concluded on an inspiring note, with Tanaya Parab's journey serving as a clear example of how engineers can make meaningful contributions to national defense. The seminar not only raised awareness about opportunities in the defense forces but also motivated students to pursue a career of service, leadership, and technological innovation.

The event underscored the need for continued engagement between engineering institutes and defense organizations. The IETE-ISF was encouraged to organize follow-up workshops, career counseling sessions, and interactions with defense personnel to maintain student interest and facilitate easier entry into the armed forces. Overall, the seminar left the students with a deep sense of purpose, instilling both pride and excitement about future possibilities

Event Pictures

3.5 Trek to Korigad Fort under IETE-SF

Faculty Members: Prof. Amit A Deshmukh, Dr. Rajendra Khavekar
Dr. Sanjay Dehsmukh ,Dr. Sunil Karamchandani, Dr. Ankita Malhotra,
Prof. Dipti Kale,Prof. Tushar Sawant

Date of the session: 25th August 2024

No. of Participants: 100

Participants: SE students, TE students & Faculty members of EXTC department.

Objectives of the activity:

- Strengthen the bonds by engaging in a physically challenging and adventurous activity, promoting teamwork, and enhancing mutual trust.
- Offer participants an exciting and fun experience to break away from the monotony of their daily routines and encouraging participants to stay fit and maintain their health.

Contents:

On the 25th of August, 2024, the IETE-ISF (Institution of Electronics and Telecommunication Engineers - Student Forum) of Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized a thrilling and adventurous trek to Korigad Fort, near Peth Shahapur, Lonavala. The event was part of the IETE-ISF's ongoing efforts to promote extracurricular activities that combine physical fitness, mental well-being, and historical education. This trek not only offered students a break from their academic routines but also provided them with an opportunity to connect with nature and each other, fostering team spirit and leadership skills.

With over 100 students from the Electronics and Telecommunication (EXTC) department participating, the event underscored the enthusiasm and adventurous spirit of the student community at DJSCE. The event was guided by experienced trek leaders and supported by faculty members, ensuring that it was both enjoyable and safe for all participants.

Event Planning and Logistics

The meticulous planning for the trek was led by Dr. Amit Deshmukh, Head of the EXTC Department, and executed by the IETE-ISF team. Early morning pick-ups were arranged at multiple locations across Mumbai, including Priyadarshini (Chembur) and the primary meeting point at Dinanath Natya Mandir in Vile Parle East. Two buses transported students and faculty to the base village of Peth Shahapur, the trek's starting point.

Participants were advised to dress in appropriate trekking attire and carry essentials such as water, snacks, and rain gear due to potential monsoon showers. Upon arrival at the base, trek leaders provided safety instructions and trekking tips, ensuring that all participants were well-prepared for the journey.

Overview of Korigad Fort

Korigad Fort, located about 20 km south of Lonavala, stands at an elevation of approximately 923 meters above sea level. The fort is a part of the Sahyadri mountain range and is known for its historical significance and stunning natural beauty. It was incorporated into Chhatrapati Shivaji Maharaj's empire in 1657, and its strategic location offered commanding views of the surrounding valleys. Today, Korigad Fort is a popular destination for trekkers who are drawn to its scenic landscapes, ancient ruins, and the serenity of its two well-preserved lakes.

The trek to Korigad is considered moderate in difficulty, making it accessible for beginners while still providing enough challenges for experienced trekkers. The route to the fort is well-marked, passing through forested areas and rocky paths that lead up to the fort's impressive stone gates. The expansive plateau at the top offers' panoramic views and a sense of history, with remnants of old structures, bastions, and cannons scattered around the fort.

The Trek Experience

Commencement of the Trek:

The trek began around 11:15 am following the group's arrival at the base village. Initially, the fog created a mystical atmosphere with low visibility and a cool breeze, adding a sense of adventure to the ascent. Guided by experienced leaders, participants navigated rocky paths and forest trails, adhering to safety protocols and following directions closely.

Summit, Exploration and Descent:

By 2:00 pm, the group reached the summit. Dense fog limited the usual panoramic views but created a surreal experience. Participants explored the fort's historic gateways, cannons, temples, and tranquil lakes, which looked almost magical in the fog.

Around 3:30 pm, the weather changed dramatically, with heavy rains making the descent challenging. The rocky paths became slippery, and thick foliage offered little protection from the downpour. Despite the difficulties, participants maintained high spirits and demonstrated remarkable teamwork, helping each other navigate the treacherous conditions. The adverse weather turned into a memorable adventure, reinforcing the group's unity.

By 4:30 pm, the group safely reached the base, drenched but satisfied. A traditional "desi style" lunch was served, offering a warm and comforting meal after the adventurous trek. This break allowed everyone to relax, dry off, and share their experiences.

Following lunch, the group prepared for the return journey, with buses departing Peth Shahapur around 5:30 pm. Reflecting on the day's events, participants agreed that the trek, despite the unexpected

weather, was an unforgettable experience. The group arrived back in Mumbai around 10:00 pm, with slight variations due to traffic.

Participant Feedback and Reflections

Feedback from the participants was overwhelmingly positive. Students appreciated the break from their academic routines and the chance to engage in a physically demanding yet rewarding activity. The slightly challenging weather conditions added a unique aspect to the trek, turning it into a true adventure that tested both their endurance and teamwork. Despite the fog and heavy rains, or perhaps because of them, the trek was seen as an unforgettable experience that provided valuable lessons in resilience and adaptability.

Participants commended the organization of the event, highlighting the clear communication, safety measures, and support provided by the trek leaders. The scenic beauty of Korigad Fort, combined with the thrill of overcoming natural obstacles, left a lasting impression. Many expressed a desire to participate in similar events in the future, seeing the trek as a valuable component of their overall educational and personal development.

Acknowledgments

The success of the Korigad trek was a result of the dedicated efforts of the IETE-ISF team, under the leadership of Dr. Amit Deshmukh, accompanied by the training and placement officer Mr Rajendra Khavekar. Special thanks are extended to the faculty members whose support ensured the smooth execution of the event, maintaining high standards of safety and organization. Their commitment to providing enriching extracurricular experiences is highly valued and essential for the holistic development of students at DJSCE.

Conclusion

The Korigad Fort trek was a resounding success, blending adventure, historical learning, and personal growth. The event highlighted the resilience and adventurous spirit of the student community, who embraced challenging weather conditions with enthusiasm and determination. This experience underscored the importance of outdoor activities in enhancing student life and fostering a deeper appreciation of cultural and natural heritage. The IETE-ISF looks forward to organizing more such events in the future, continuing to promote a well-rounded and enriching environment for all its members.

Photographs of the Event:

Outcomes:

- The event successfully fostered a stronger sense of unity and collaboration among the participants. The shared experience of conquering the trek's challenges created lasting bonds among the participants.
- The trek encouraged a culture of active living and physical fitness within the college community. Participants were motivated to challenge their physical limits, and this awareness of the importance of fitness is likely to have a lasting impact on their overall well-being.
- The inclusion of team-building activities during the trek encouraged problem-solving and teamwork among participants. These activities strengthened participants' ability to collaborate effectively and address challenges collectively.

3.6 Trek to Rajgad Fort under IETE-SF

Faculty Members: Prof. Amit A Deshmukh, Dr. Sanjay Dehsmukh, Dr. Sunil Karamchandani, ,Prof. Tushar Sawant

Date of the session: 19th to 20th October 2024

No. of Participants: 40

Participants: SE students, TE students & Faculty members of EXTC department.

Objectives of the Activity:

- Encouraging Holistic Development
- Teamwork and Leadership
- Skill Development
- Encouraging Creativity and Innovation

Content:

On 20th October 2024, the IETE-ISF (Institution of Electronics and Telecommunication Engineers - Student Forum) from Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized an exciting and physically challenging trek to Rajgad Fort, one of Maharashtra's most historically significant landmarks. The event was organized to encourage a balance between academics, physical health, and exploration of the local heritage.

Rajgad Fort, once the capital of Chhatrapati Shivaji Maharaj's empire, provided a stunning backdrop for this adventure. The trek offered students a chance to step out of their daily routines, connecting with nature and their peers in a setting that emphasized endurance, collaboration, and leadership.

The participation of over 40 students from the Electronics and Telecommunication (EXTC) department showcased the vibrant enthusiasm of the DJSCE student body. The trek had faculty members accompanying the group to ensure a well-organized and safe experience for everyone. Students not only enjoyed the scenic trek but also gained insights into the historical importance of the fort.

Event Planning and Logistics

The successful planning of the trek to Rajgad Fort was orchestrated by the enthusiastic IETE-ISF team, along with Prof. Amit Deshmukh, Head of the EXTC Department. To accommodate participants, late night pick-ups were arranged at various strategic locations across Mumbai, including Priyadarshini in Chembur and the primary meeting point at Dinanath Natya Mandir in Vile Parle East. A bus was utilized to transport students and faculty to the base village, the starting point of the trek. Participants were advised to wear suitable trekking attire and to carry essential items such as water, snacks, and rain gear, anticipating possible monsoon showers, though none were encountered on the actual trek.

Overview of Rajgad Fort

Rajgad Fort, perched at an elevation of approximately 1,395 meters (4,580 feet), is a captivating trekking destination that offers both adventure and a glimpse into Maharashtra's rich history. Known for its strategic significance as the capital of Chhatrapati Shivaji Maharaj's empire, the fort boasts stunning panoramic views of the surrounding Sahyadri mountain range.
The trek typically begins at the base village of Gunjavane, which is accessible by road. The journey to the base village involves scenic routes through lush green landscapes, especially vibrant during the

monsoon season.
The trek is classified as moderate, suitable for individuals with a basic level of fitness. While the ascent can be steep and challenging in places, it is manageable for most trekkers, with several resting points along the way. As you trek, you will encounter remnants of the fort's historical architecture, including impressive gates, watchtowers, and water cisterns, offering insights into its past.
Once at the top, trekkers are rewarded with breathtaking views of the Sahyadri range and surrounding valleys. The fort encompasses several structures to explore, including the Padmavati Machi, the *Ballekilla* (the highest point), and the ruins of the royal palace, each narrating stories of the Maratha Empire.

The Trek Experience

Commencement of the Trek:

The journey began with the group departing from Vile Parle at 12:30 AM, traveling overnight to reach the base village of Rajgad Fort by 7:00 AM. After a hearty breakfast and time to freshen up, the group geared up for the climb and began by 9:00 AM. Accompanied by our trek leader, the participants navigated through uneven terrain and rocky trails, prioritizing safety and carefully following all given directions.

Ascent, Summit, Exploration and Descent:

The ascent commenced shortly after breakfast. The participants navigated the rocky paths and lush forest trails under a hot and sunny sky. The warm weather made it essential to stay hydrated, and trekkers refreshed themselves with plenty of water, cucumbers and lemonade along the way. They reached the 'Chor Darvaja' by 11:00 AM.
The climb to the summit had stops along places like the Padmavati temple, Ballekilla along the way which entranced everyone.
By 3:00 PM, the group reached the summit, the Suvela Machi. Although the clear skies provided stunning views, the heat added to the challenge of the trek. Participants explored the fort's historic gateways, cannons, temples, and scenic flower beds, all showcasing the beauty of Rajgad.
The descent began in the afternoon, with the sun shining brightly. By 5:00 PM, the group safely returned to the base, feeling accomplished and invigorated. A late lunch was served in the village, where participants enjoyed a well-deserved meal while sharing stories and reflecting on the day's adventures. The trek proved to be an unforgettable experience filled with camaraderie, exploration, and the thrill of nature.Everyone arrived back in Mumbai around 12:00 pm.

Participant Feedback and Reflections

The response from participants was overwhelmingly enthusiastic. For many, the trek was a welcome escape from their academic schedules, providing an opportunity to embrace physical exertion and connect with nature. The sunny weather, though intense, added an extra layer of excitement and challenge, pushing everyone to work together and support one another. The trek became an unforgettable adventure that tested their endurance and highlighted the importance of collaboration.

Students were particularly impressed with the seamless organization of the event, noting the clear guidance, well-implemented safety precautions, and strong support from the trek leader. The majestic beauty of Rajgad Fort, combined with the satisfaction of overcoming the rugged terrain, left a deep impact on everyone involved. Numerous participants expressed a keen interest in joining future treks,

viewing the experience as both a valuable learning opportunity and a key aspect of their personal growth.

Acknowledgments

The Rajgad trek's success can be attributed to the tireless efforts of the IETE-ISF team, under the leadership of Prof. Amit Deshmukh, Head of the EXTC Department, and with the key support of Mr. Rajendra Khavekar, the training and placement officer. A special note of gratitude goes to the faculty members, whose dedication and involvement were instrumental in executing the event seamlessly, ensuring safety and organization were upheld at every step. Their unwavering commitment to offering students enriching extracurricular opportunities is vital for fostering the all-round development of the DJSCE community.

Conclusion

The Rajgad trek organized by IETE-ISF was a resounding success, offering participants not only an adventurous escape from their academic routines but also an opportunity for personal growth. The combination of physical endurance, team collaboration, and historical exploration provided a well-rounded experience that left a lasting impression on everyone involved. Trekking to Rajgad Fort is not just about reaching the summit; it's an enriching experience that combines physical activity with a deep appreciation for Maharashtra's cultural heritage. The journey provided trekkers with a sense of achievement, connection to nature, and an opportunity to reflect on the fort's historical significance amidst its stunning landscapes.The event's seamless execution, thanks to the leadership and support of the organizing team and faculty members, ensured that it was both safe and memorable. This trek stands as a testament to the value of extracurricular activities in fostering resilience, leadership, and camaraderie, and IETE-ISF looks forward to more such enriching experiences in the future.

Event Pictures

3.7 En-Core 1.0

Faculty Members: Prof. Amit A Deshmukh, Dr. Poonam Kadam, Dr. Satishkumar Chavan Dr. Sanjay Dehsmukh, Dr. Sunil Karamchandani, Prof. Rahul Taware, Prof. Pavankumar Borra, Dr. Ankita Malhotra, Prof. Supriya Dicholkar, Prof. Dipti Kale

Date of the session: 28th September 2024

No. of Participants: 200

Participants: SE students, TE students & Faculty members of EXTC department.

Introduction

On September 28th, 2024, the IETE-ISF of Dwarkadas J. Sanghvi College of Engineering hosted its first-ever analog hardware hackathon: En-Core 1.0. This ground breaking event marked a milestone for the EXTC department, offering over 200 students a unique opportunity to develop and showcase their hardware and software skills. The hackathon, specifically designed for EXTC students, aimed to push participants beyond theoretical learning, encouraging hands-on innovation in an intense, 8-hour competitive environment.

The event not only served as a platform to challenge participants' creativity and problem-solving abilities but also emphasized the practical application of classroom knowledge in a real-world setting. En-Core 1.0 was an important step toward fostering a culture of hardware design and innovation within the department.

Round Structure

1. Pre-Event Stage

The Pre-Event Stage, held from September 21st to 26th, 2024, was designed to shortlist the top 40 teams for the main event. This stage consisted of two major components:

Quiz (35 marks): Conducted via Google Forms, this tested participants' theoretical knowledge on key topics relevant to analog hardware design.

KiCAD Work (45 marks): Participants submitted their work via GitHub, which included:

Schematic Design (10 marks)

Simulation (15 marks)

PCB Design (15 marks)

GitHub Hosting with team credits (5 marks)

Teams were evaluated on their theoretical knowledge and their ability to apply it in a practical setting, with a total score out of 80 marks. The top teams were selected based on the accuracy, efficiency, and quality of their submissions, ensuring that the most capable teams progressed to the main event.

2. Main Event (Event Day)

On September 28th, 2024, the selected 40 teams competed in the 8-hour hackathon, where they were tasked with developing a functional analog hardware model on a breadboard. The problem statement was revealed at the beginning of the event, challenging the participants to think quickly and act efficiently

During the event, teams were assessed on the following criteria:

- Functionality of the breadboard model
- Design quality of the schematic and PCB, submitted via GitHub
- Debugging and troubleshooting skills

Participants had to demonstrate their ability to convert the problem statement into a working model while adhering to time constraints. The judges evaluated the teams on the technical accuracy, creativity, and robustness of their hardware designs. The final submissions were a testament to each team's technical proficiency and ability to innovate under pressure.

Event Timeline

- September 21st - 26th, 2024: Pre-event stage (Quiz and KiCAD submissions via GitHub).
- September 27th, 2024: Announcement of shortlisted teams for the main event.
- September 28th, 2024: Main Event (problem statement disclosure, breadboard development, testing, and final design submissions).

Judging and Evaluation

Judging in the Pre-Event Stage was based on the teams' theoretical understanding and practical skills in KiCAD, with special emphasis on the completeness and accuracy of their schematic designs, simulations, and PCB layouts. Only the teams that demonstrated a strong combination of theoretical and hands-on skills advanced to the main event.

In the Main Event, participants were evaluated on their ability to develop a functional breadboard model within the allotted 8 hours. The judging criteria included:

- Functionality: How well the final hardware model operated.
- Design: Quality and innovation of the schematic and PCB designs submitted via GitHub.
- Debugging: Teams' ability to troubleshoot and resolve problems in real time.

The teams that excelled in these areas displayed exceptional problem-solving abilities and technical proficiency, standing out among their peers.

Winners and Prizes

The following teams emerged victorious after a challenging day of competition:

- Team 13: Soham Lotlikar, Dhruv Bhaip, Sahil Pisal, Shantanoo Aher
- Team 31: Tanishq Patel, Varun Choudhary, Soham Shenoy, Swayam Bhosale
- Team 37: Gargeya Parab, Adit Shah, Soham Hanchate, Rishab Sharma

Each of these teams demonstrated remarkable creativity, attention to detail, and technical skill, earning them recognition for their outstanding work. The event featured a ₹10,000 prize pool, distributed among the top teams.

Conclusion:

The success of En-Core 1.0 marked an important milestone for the EXTC department, highlighting the

talent and creativity of its students. This inaugural event fostered a spirit of innovation and collaboration, encouraging participants to push their boundaries in the field of hardware design. By providing a platform for real-world problem-solving, the event proved that hands-on learning is critical to developing future engineers.

Thanks to the efforts of the organizing committee and the enthusiastic participation of students, En-Core 1.0 ran smoothly and delivered an impactful experience for all involved. With over 200 participants and a ₹10,000 prize pool, this hackathon has firmly established itself as a key event within the department. The success of this edition has set a strong foundation for future iterations, inspiring students to continue exploring and innovating in the field of analog hardware design.

Event Pictures


DWARKADAS J. SANGHVI

3.8 Board of Studies Meeting

The Board of Studies meeting of Department of Electronics and Telecommunication Engineering was conducted in a hybrid mode on Thursday, 30th November, 2024 at 3 pm onwards in the conference room, DJSCE. The meeting was held to discuss and approve:

1. Minutes of meeting of 8th BOS meeting held on 21/04/2023.
2. Approval of DJS22 detailed syllabus of semester V and VI and Honors/Minor Degree Program, in semester VI & VIII subjects.
3. Approval of change in oral/practical Evaluation scheme to only oral for Honors Degree Program in the subject of Intelligent Connectivity: 5G and IoT, semester VI and Minor Degree course in Industry 4.0, in semester VII & VIII.
4. To approve the panel of paper setters and examiners for various exams to be held under DJS19 and DJS22 scheme for UG program in semester III-VIII & PG program in semester III & IV for the exam to be conducted from December 2023 onwards.
5. To approve NPTEL credit course guidelines for PG program.
6. To appoint examiner for M. Tech student towards the conduction of Dissertation stage II exam in his fourth semester.
7. Proposed NEP 2020 curriculum, DJS23 scheme.

The meeting was attended by the BOS members Dr. Jayakrishnan Nair, Dr. K. P. Ray, Dr. Sunil Kopparapu, Dr. S. S. Mande and faculty members of the EXTC Department.

Following were the points discussed and the suggestions provided: --

(i) Minutes of meeting of 8th BOS meeting were approved.

(ii) The UG DJS22 detailed syllabus for semester VII & VIII and Honors/Minor Degree Program semester VII -VIII subjects were presented for the approval. The suggestions made in the proposed syllabus of DJS22 curriculum are as follows:

a) Dr. K.P. Ray suggested to include "GaN based solid state microwave generation devices" in MWE semester VII course of DJS22.

b) Dr. K.P. Ray recommended to add "Introduction of 6G" in Mobile Communication semester VII course of DJS22.

c) It was suggested by Dr. K.P. Ray to include real case applications of Embedded systems in last module of the course Embedded Systems in semester VII.

d) Suggestion was made by Dr. Sudhakar Mande and Dr. K.P. Ray regarding "renaming of Advanced VLSI course as Analog VLSI" based on its contents.

e) Dr. K.P. Ray advised to appropriately rename the course Microwave amplifier and

oscillator design.

(iii)The original and Proposed DJS23 scheme of semester V & VI was discussed and the overview of the contents of the respective courses were presented. The course details for the semester V & VI of DJS23 scheme will be prepared and discussed in the next BOS meeting.

(iv) Exemption of two courses (Liberal Learning & FE program core course) for the drop out students enrolling from one scheme to another was approved. The final equivalence course structure will be presented for approval in the next BOS meeting.

(v) Examiner panel for DJS22 & DJS23 UG curriculum and PG program was presented and approved by the committee.

The meeting concluded with vote of thanks to all the members attended.

Prof. Sheeja Nair Autonomy Coordinator EXTC Dept., DJSCE	Dr. Poonam A. Kadam Autonomy Coordinator EXTC Dept., DJSCE	Prof. Amit A. Deshmukh Professor & Head EXTC Dept., DJSCE

3.9 Pre-Placement Activities

The goal of these activities is to improve the employability of final-year and pre-final-year students by organizing a series of pre-placement events. These activities are designed to provide students with the skills, knowledge, and confidence they need to succeed in campus placement drives and land their dream jobs.

These activities include:

1. Skill Development Workshops (Technical and Soft Skills)
2. Resume Building Sessions
3. Mock Interviews and Group Discussions
4. Aptitude and Technical Test Preparation
5. Industry Interactions and Networking
6. Career Counselling and Guidance

Based on the feedback received from the alumni and the industrial experts, these activities are proposed and planned by the Faculty Placement Coordinators of the Electronics and Telecommunication Department Dr. Aarti G. Ambekar and Prof. Tushar Sawant, along with the Student's Placement Coordinators under the guidance of Prof. Amit A. Deshmukh (Prof. and Head EXTC Department) and Dr. Rajendra Khavekar (TPO, DJSCE).

Few of the activities are conducted in the first half of AY 2024-2025. The in depth reports of the same are as given below.

Sessions on *Object Oriented Programming*

Speaker: Prof. Nancy Nadar

Association of the Speaker: Assistant Professor, Department of Computer Engineering, DJSCE, Mumbai

Dates of the Sessions: 10th August, 24th August and 31st August, 2024.

Venue: DJSCE EXTC Department

No. of Participants: 100+ Participants (Third Year Students)

This session was introduced as a discussion on Object-Oriented Programming (OOP). The speaker, Prof Nancy Nadar, assistant professor in the computer department, has extensive experience in the field of OOPS and various other programming languages such as C/C++, Java, Python, etc. She has a master's degree and has industry experience in the said topic. The primary goal of the session was to cover the basics of Object Oriented Programming [OOPs] and explore their practical applications in the industry

Covering overview of Object-Oriented Programming (OOP) in Java Topics:

Prof. Nancy Nadar delivered an insightful overview of key Object Oriented Programming[OOPs] concepts, focusing on their practical relevance in real-world scenarios. She emphasized the importance of mastering the underlying logic behind OOPS, rather than being restricted by programming languages. The discussion covered versatile topics and foundation of OOPS concepts such as encapsulation, inheritance, polymorphism, etc. and their implementations, all aimed at enhancing problem-solving skills. Some of the topic that were covered were as follows:

Here's an overview of Object-Oriented Programming (OOP) in Java in simplified points:

- ***Encapsulation***
  - Bundles data (attributes) and methods (functions) into a single unit (class).
  - Controls access to data through access modifiers (private, public), using getter and setter methods.
  - Helps protect data integrity and improve modularity.

- ***Inheritance***
  - Enables new classes to inherit features (fields and methods) from existing classes.
  - **Promotes code reusability by allowing a subclass to extend a superclass.**
  - **Uses the extends keyword to establish relationships between classes (e.g., class Bike extends Vehicle).**
- ***Polymorphism***
  - Allows objects to be treated as instances of their parent class, improving flexibility.
  - Achieved through:
    - **Method Overloading**: Multiple methods with the same name but different parameters within the same class.
    - **Method Overriding**: A subclass provides a specific implementation for a method already defined in the superclass.
- ***Abstraction***
  - Hides unnecessary implementation details, focusing only on essential features.
  - Achieved through:
    - **Abstract Classes**: Classes that can't be instantiated and often have abstract methods.
    - **Interfaces**: Define a contract for classes to implement, ensuring specific methods are included without detailing how they work.

- ***Method Overriding***
  - Method overriding is used in runtime polymorphism. When a child class overrides a parent class's method, the child class might offer an alternative implementation.

❖ **Method Overloading**

- Method overloading is used in Compile Time Polymorphism. Although two methods or functions may have the same name, the number of arguments giveninto the method call may vary. Therefore, depending on the number of parameters entered, you may obtain different results.

Together, these principles create a structured, maintainable, and reusable approach toprogramming in Java, C++ and various different Object Oriented Programming languages. The session on Object Oriented Programming [OOPs] led by Prof. Nancy Nadar concluded with a strong emphasis on practical understanding and real-world applications. Engaging around 150 students, Prof. Nancy underscored the significance of focusing on logical reasoning rather than getting bogged down by language-specific implementations. Through examples of explaining a class as a family to explain the hierarchy of a parent and a child class also through this example she explained method overloading and overriding—she made complex concepts accessible and relatable. Her encouragement for students to learn from others' solutions and gradually take on more challenging problems left them inspired to pursue continuous improvement in their academic and professional end devours. Overall, the session was a valuable experience, equipping students with the tools and mindset needed for success in the field of OOPs.

A Session On *Data Structures and Algorithms (DSA) from a Placement Perspective*

Speaker: Prof. Pranit Bari
Association of the Speaker: Assistant Professor, Department of Computer Engineering, DJSCE, Mumbai
Date of the Session: 9th October, 2024
Venue: MS Team
No. of Participants: 80+ Participants (Third Year Students)

This session was introduced as a discussion on data structures and algorithms (DSA) from an industry perspective. The speaker, Prof. Pranit, has extensive experience in the field. He has a master's degree and has published books on data structures in Python and C. The primary goal of the session was to cover the basics of DSA and explore their practical applications in the industry.

Covering core Data Structure and Algorithm Topics:

Prof. Pranit Bari delivered an insightful overview of key data structures and algorithms (DSA) concepts, focusing on their practical relevance in real-world scenarios. He emphasized the importance of mastering the underlying logic behind DSA, rather than being restricted by programming languages. The discussion covered versatile topics, including stacks, queues, linked lists, and their implementations, all aimed at enhancing problem-solving skills. Some of the topic that were covered were as follows:

1. **Versatility of Data Structures**: Prof. Pranit emphasized that data structures can be implemented in a variety of programming languages. The speaker however highlighted that the key to success lies in understanding the logic and ideas behind the solutions, rather than being limited to language-specific implementations. Data structures were classified into two broad categories: linear (e.g., linked lists) and non-linear (e.g., graphs, trees), with the latter being more useful for solving complex problems.

2. **The Stack Data Structure:** This topic followed a last-in-first-out (LIFO) approach. Real-world applications of stacks, such as the back button in web browsers, were

3. discussed to illustrate their practical relevance. Prof. Pranit explained the standard functions of push and pop, stressing the importance of adhering to the predefined function definitions rather than modifying them, as this is the industry standard.

4. **Implementing Stacks with Arrays:** The session explored the implementation of stacks using arrays, emphasizing the importance of handling edge cases such as a full stack or an empty stack.

The process of deleting an element from a stack was discussed in detail, covering scenarios where the element to be deleted is at the beginning, middle, or end of the stack.

5. **Queues and Stacks:** The attendees were introduced to the concept of implementation a queue using a stack data structure. This approach requires the use of two stacks to maintain the first-in-first-out (FIFO) principle of a queue. The speaker walked through the logic of performing enqueue and dequeue operations using the stack data structure.

6. **Binary Conversion using Stacks:** Prof. Pranit presented a problem of converting a given number to its binary representation using a stack. The step-by-step approach, involving repeatedly dividing the number by 2 and pushing the remainders onto the stack, was explained in detail. The speaker then demonstrated an alternative solution without using a stack, relying on mathematical operations to achieve the same result.

7. **Linked Lists and Node Deletion:** The session introduced the linked list data structure, explaining the concept of nodes and the use of pointers to connect them. The process of deleting a node from a linked list was discussed in detail, considering various scenarios, such as deleting the first, middle, or last node, as well as the case where the value to be deleted is not present in the list.

8. **Reversing Linked Lists:** Prof. Pranit demonstrated the logic for reversing a linked list without using a stack. The approach involved using three pointers (current, next, and previous) to iteratively update the links between the nodes, effectively reversing the order of the list.

Development of Problem-Solving Skills:

Prof. Pranit laid out the following advice for the students:

- **Practice is Key to Problem-Solving:** Regular practice is essential for developing strong logical thinking and problem-solving skills. Platforms like LeetCode and CodeChef offer a wide range of problems, from easy to challenging, that can help you build your skills in data structures and algorithms. Start with simpler problems to establish a foundation and gradually work your way up to more complex ones. This gradual progression will allow you to build your confidence and understanding.
- **Learn from Others' Solutions:** Comparing your solutions to those of others can be a valuable learning experience. By examining different approaches to a problem, you can gain insights into alternative methods, identify areas for improvement in your own solutions, and learn new

techniques. It's important to be open-minded and willing to learn from others, even if their solutions differ significantly from your own.

- **Continuous Improvement:** Problem-solving is a skill that requires constant practice and improvement. Don't be afraid to challenge yourself with increasingly difficult problems and seek out new opportunities to learn and grow. By consistently pushing yourself outside of your comfort zone, you can develop the skills and confidence needed to tackle complex problems and succeed in your career.

The session on data structures and algorithms (DSA) led by Prof. Pranit concluded with a strong emphasis on practical understanding and real-world applications. Engaging around 85 students, Prof. Pranit underscored the significance of focusing on logical reasoning rather than getting bogged down by language-specific implementations. Through illustrative examples such as using web browsing to explain stacks and employing binary conversions to clarify queues and linked lists, he made complex concepts accessible and relatable. His encouragement for students to learn from others' solutions and gradually take on more challenging problems left them inspired to pursue continuous improvement in their academic and professional endeavors. Overall, the session was a valuable experience, equipping students with the tools and mind set needed for success in the field of DSA.

Mock Aptitude Test and Technical Test for the Placements

Organized by: Placement Team of EXTC Department

Venue: Online Platforms like: Ms Team and HackerRank

Participants: Third Year Students

The primary goal of the Mock Aptitude and Technical Test was to prepare students for upcoming campus placement drives by familiarizing them with the test patterns, improving their problem-solving skills, and assessing their readiness for competitive recruitment processes. The Mock Aptitude Test is designed to prepare students for campus placements by simulating real recruitment exams. Covering key areas like quantitative aptitude, logical reasoning, and verbal ability, it gives students a feel for the types of questions, time constraints, and pressure they'll face in actual tests. This activity not only helps students identify strengths and areas for improvement but also builds their confidence for upcoming placement drives, enhancing their overall readiness for technical and non-technical roles.

Test Structure

Aptitude Test

- **Topics Covered:**
  - Quantitative Aptitude (Time and Work, Percentages, Profit and Loss, Ratios, etc.)
  - Logical Reasoning (Puzzles, Seating Arrangements, Blood Relations, etc.)
  - Verbal Ability (Comprehension, Grammar, Sentence Completion, etc.)
- **Duration:** [45 Mins]
- **Number of Questions:** [25]

Technical Test

- **Topics Covered:**
  - Core Subjects ([e.g., Data Structures and Algorithms, Programming Languages, etc.])
  - Problem-Solving/Programming ([e.g., Coding Problems in C, Python, etc.])
- **Duration:** [45 Mins]
- **Number of Questions:** [25]

In these tests activities, Test 1 was the Aptitude Test, focusing on areas like quantitative aptitude, logical reasoning, and verbal ability to assess students' foundational skills. While the test 2, was the Coding Test, evaluating the programming skills, problem-solving abilities, and technical knowledge essential for roles that require coding proficiency. Together, these tests give students a comprehensive

preparation experience, enhancing their readiness for varied aspects of recruitment processes.

Thus the overall performance was promising, with noticeable strengths in Logical Reasoning and Quantitative sections, but room for improvement in Verbal Ability and select technical areas. The Mock Aptitude and Technical Test proved to be a valuable exercise for students, giving them insights into their strengths and weaknesses. It also provided a clear roadmap for further preparation. Continued efforts in this direction will significantly enhance placement success rates.

4. ACHIEVEMENTS

4.1 Faculty Publications- Conferences / Journals

Journal publication

Sr.No	First Author	Paper Details	Indexed by
1	Prof. Amit Deshmukh	Deshmukh, A. A., Manek, J., & Ambekar, A. G. (2024). Circularly Polarized Variations of Truncated Corner Square Microstrip Antennas Employing a U-slot. IETE Journal of Research, 1–12. https://doi.org/10.1080/03772063.2024.2426698	SCOPUS
2	Dr. Venkata A. P. Chavali	Venkata A. P. Chavali, and Amit A. Deshmukh, "Multi Resonant Gap-Coupled Designs of E-Shape Microstrip Antenna for Wideband Response," *Progress In Electromagnetics Research C*, Vol. 149, 67-79, 2024. doi:10.2528/PIERC24092002	SCOPUS
3	Supriya Dicholkar	Supriya Dicholkar, & Jagannath Nirmal. (2024). A Novel Feature Reduction Technique for Detection of DoS Attack on Dataset. International Journal of Communication Networks and Information Security (IJCNIS), 16(3). https://doi.org/10.17762/ijcnis.v16i3.6715	SCOPUS
4	Dipti H. Kale	Dipti H. Kale, Emotion Recognition from Children Speech – A Review International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 http://www.ijert.org IJERTV13IS080064 (This work is licensed under a Creative Commons Attribution 4.0 International License.) Published by : Vol. 13 Issue 08, August-2024	UGC
5	Supriya Dicholkar	S. V. Dicholkar and J. H. Nirmal, "DoS Attack Detection Using Feature Selection with Information Gain and ML Classification," *2024 Second International Conference on Advances in Information Technology (ICAIT)*, Chikkamagaluru, Karnataka, India, 2024, pp. 1-6, doi: 10.1109/ICAIT61638.2024.10690842.	IEEE
6	Supriya Dicholkar	Dicholkar, S., Nirmal, J.H. (2024). Comprehensive Analysis of Different Boosting Techniques for Attack Detection in IoT Network. In: Patil, M., Vyawahare, V., Birajdar, G. (eds) Intelligent Computing and Big Data Analytics. ICICBDA 2024. Communications in Computer and Information Science, vol 2235. Springer, Cham. https://doi.org/10.1007/978-3-031-74701-4_10	Springer

4.2. Interaction of faculty with outside world

FDP/ STTP/Webinar/Workshop attended by Faculty Members:

Sr. No.	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Prasad S. Joshi	attended one-day workshop organized by UGC at IIM - Ngp, along with Principal, Dr. Hari Vasudevan and NEP implementation committee member - Dr. Atul Dhale on	23rd October 2024.
2	Dr. Ankita Malhotra	attended workshop on RaoS-Phased array and reflector antenna design and analysis	22nd July 2024.
3	Prof. Abhilasha Raghtate	attended FDP on 'Recent Trends in Technology".	26th August to 28th August 2024.
4	Prof. Abhilasha Raghatate, Dr. Ankita Malhotra, Prof. Supriya Dicholkar.	attended 10 Hours International Faculty Development Program on AI And Gen AI with Industry Application.	16th July to 22nd July 2024.
5	Supriya Dicholkar	attended one week ISTE approved STTP on Research Funding, Publications, and IPR: A Journey from Fundamentals to Advanced Methodologies	from 10th June to 14th June 2024.
6	Prof. Dipti Kale	attended one week FDP ON AI INTEGRATION WITH HEALTHCARE AND BANKING	From 12th December to 18th December 2024
7	Prof. Bahar C. Soparkar	attended ISTE approved FDP on Effective AI tools Enhancing Teaching, Learning and Research	From 1st July 2024 to 6th July 2024

4.3. NPTEL/COURSERA Courses completed by faculty members:

Sr.No	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Poonam Kadam.	NPTEL -8 Weeks- Microelectronics: Devices to Circuits	November 2024.
		NPTEL-4 week- TOPPER (Silver Medal) for course "Fundamentals of Electronic Device Fabrication"	August 2024.
		NPTEL-8 week- TOPPER (Silver Medal) for course "Research Methodology"	November 2024.
2	Yukti Bandi	NPTEL -8 week -got the recognition of NPTEL Topper of course "Introduction to Machine learning "	August 2024.
3	Archana Chaudhari	NPTEL -8 week -"Introduction to Machine learning" (Silver Elite certificate)	September 2024.
4	Mrunalini Pimpale	NPTEL -8 week -"Introduction to Machine learning" (Silver Elite certificate) in September 2024.	September 2024.
5	Abhilasha Raghtate	NPTEL -8 week recognition of ELITE + SILVER in Developing Soft Skills and Personality	November 2024.
		NPTEL -12 week ELITE + GOLD in Applied Linear Algebra for Signal Processing, Data Analytics and Machine Learning in November 2024.	November 2024.
6	Supriya Dicholkar.	NPTEL -12 week -"Fundamentals of Wireless Communication"	September 2024.
7	Dr. Ankita Malhotra	NPTEL -8 week -Silver medal in NPTEL course on "Introduction to Internet of Things ")	September 2024
8	Dipti Kale	NPTEL -8 week "Industrial IoT" (Silver Elite certificate).	September 2024.
9	Dr. Satishkumar Chavan	NPTEL -8 week recognition of ELITE + SILVER in Developing Soft Skills and Personality	November 2024.
10	Dr. Sunil karamchandani	NPTEL -12 week -" 5G Wireless standard Design"	Jul-Oct 2024
		NPTEL -12 week -" Introduction to Internet of Things"	Jul-Oct 2024

4.4. Faculty Achievements

Name of Faculty	Event description	Date
Prof. Amit A Deshmukh, Dr. Venkata A P Chavali, Dr. Aarti Ambekar, Prof. Tushar Sawant	granted patent on with title COMPACT WIDEBAND GAP-COUPLED VARIATIONS OF HEXAGONAL MICROSTRIP ANTENNAS ON THINNER SUBSTRATE	21st November 2024.
Dr. Prasad S. Joshi	worked as Panel Member for Personal Interview Process - PhD in Engineering and Technology Management 2024	29th June 2024
	BoS member at department of E&TC, Thakur College of Engineering and Technology, Kandivali, Mumbai	15th June 2024.
	Vice-Chancellors Nominee as Subject Expert – Electronics & Computer Science	26th June 2024.
	invited to join online BOS meeting of E&TC department, TCET	30th November 2024.
	resource Person - One-day workshop, at Parle Tilak Vidyalaya Association's Sathaye College, on PCB Design & Fabrication, for M.Sc. and B.Sc. students	21st September 2024
Dr. Vishakah Kelkar	got recognition as Active SPOC certificate from NPTEL	Jan-April 24.
Dr. Poonam Kadam	attended Industrial Training from Academy of Skill Development.	1st June to 30th June 2024.
	recognized as a reviewer for Progress in Electromagnetics Research Journals, Microwave and Optical Technology Letter	Oct/Nov 2024.
	recognized as a reviewer for PIER Journals	November 2024.
	Conducted workshop on VLSI Design Flow & Integration with FPGA	1st October 2024
Dr. Sunil Karamchandani , Prof. Ranjushree Pal & Dr. Satish Chavan	conducted workshop in collaboration with IETE-SF on MATLAB Programming for SE & TE students.	20th to 23th of August 2024
Dr. Aarti G Ambekar	as reviewer for IEEE Access journal	November, 2023
Archana Chaudhari	worked as Session chair for the 2nd International Conference on Emerging Trends in Engineering and Medical Sciences (ICETEMS 2024) organized by Yeshwantrao Chavan College of Engineering	23rd November 2024.
Dr. Ankita Malhotra	worked as reviewer for International Journal of basic and advanced research in August 2024.	August 2024.
	attended one day IEEE Bombay section Research Colloquium Series 2024.	27th July 2024.
Yukti Bandi	completed the Internship Program at Ardent Software on Data Science, AI, Machine Learning using Python (Project Based)	August 9, 2024 to September 8, 2024.
Supriya Dicholkar	worked as reviewer for frontiers in Applied Mathematics and Statistics.	June 2024.

4.5. Student's participation in various events

DJS ANTARIKSH Team achievements

DJS Antariksh is the official Martian Rover Team of Dwarkadas J. Sanghvi College of Engineering, Mumbai, India established in 2019-20. The team consists of 50 passionate 2nd and 3rd year undergraduate students from diverse engineering disciplines who are united by a shared mission to push the boundaries of space exploration through innovation. The team's motto, 'To Decipher Unimaginable', embodies its commitment to space exploration. The team aims to represent India at various international competitions like the European Rover Challenge and International Rover Challenge, showcasing its commitment to advancing space exploration by developing cutting-edge autonomous Martian rover technology.

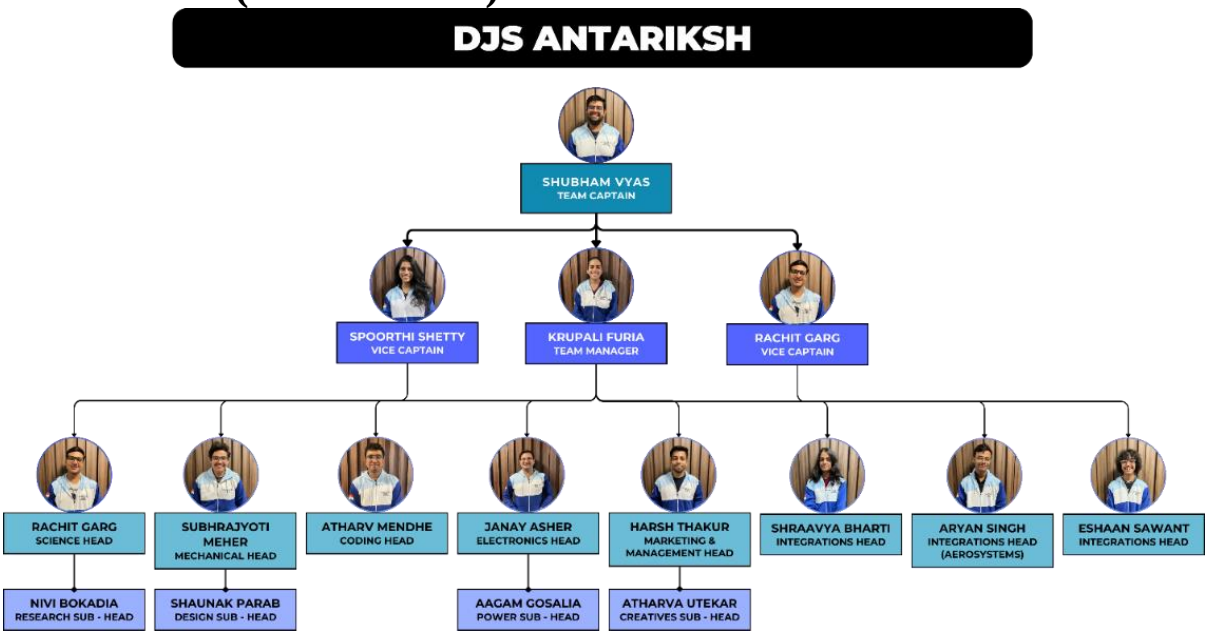
The team comprises of five departments: Electronics, Mechanical, Coding, Science, and Marketing, each contributing significantly to both technical and non-technical aspects of its operations. The team comprises of members with expertise across a broad spectrum of fields, including but not limited to Robotics, PCB and Circuit Design, Artificial Intelligence (AI) and Machine Learning, Additive Manufacturing and 3-D Design.

Team's Creations

ABHYAAN
(Team's Rover for ERC 2023 and IRC 2024)

PRAYAAN
(Team's Rover for IRC 2023)

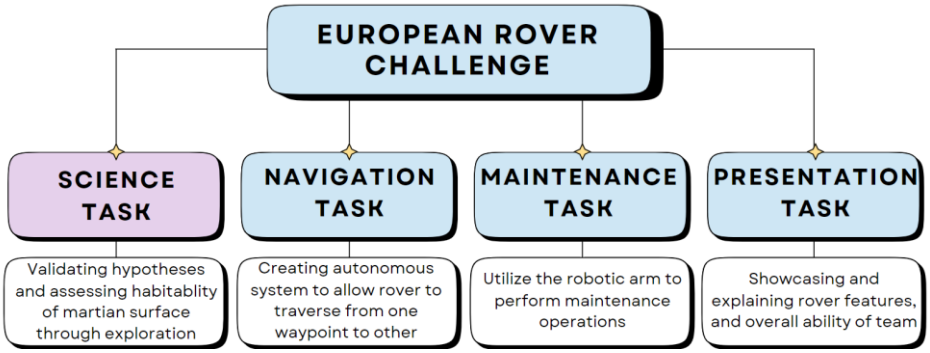
Team Structure (A.Y. 2024-25)



Competitions

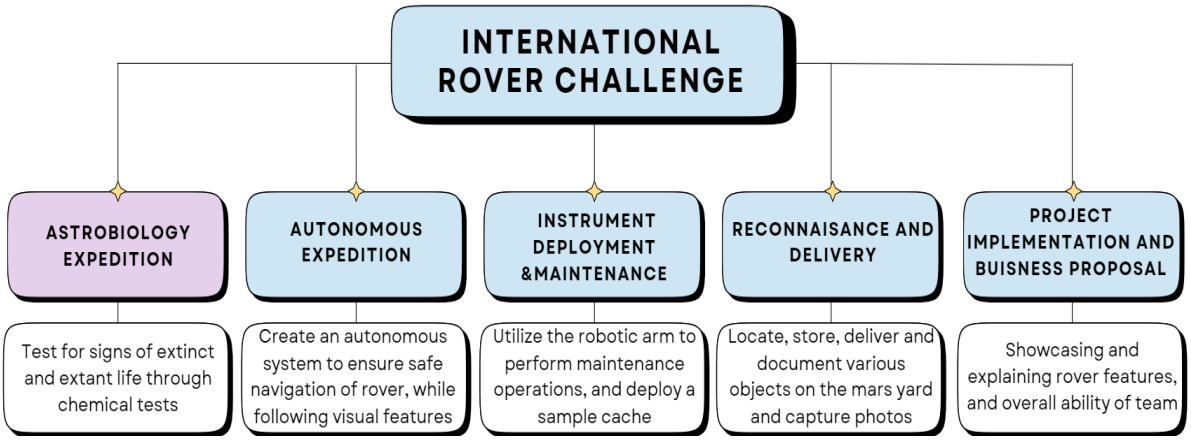
1. European Rover Challenge

The European Rover Challenge organised by the European Space Foundation takes place every year in Poland. It is an integrated programme working towards technological developments, specifically those in GPS-denied environments, with space exploration and utilisation as the leading theme. The ultimate goal of the ERC is to become a standardised test trial and benchmark for planetary robotic activities, coupled with strong professional career development platform. The competition is divided into 2 formulas: On-site and Remote.



2. International Rover Challenge

The International Rover Challenge is an international competition organised by the Space Robotics Society. It challenges university students to conceptualise, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business planning and project management.



3. International Rover Design Challenge

Space Robotics Society

International Rover Design Challenge (IRDC) is an online space engineering design and research competition by Space Robotics Society. It challenges university students to conceptualize and design Next-Gen Mars Rovers, which shall be fully equipped and mission ready for future astronaut-assistive exploration operations on Mars. Teams are supposed to carefully plan each sub-system of the Rover considering various extra-terrestrial parameters in design. This online research-oriented competition is designed for students to explore their mind and spark the innovative design thinking of individuals, free from constraints on available physical resources

Team's Achievement 2024

- **International Rover Challenge 2024**
  3rd Position Worldwide
- **International Space Drone Challenge 2024**
  2nd Position Worldwide
- **European Rover Challenge 2024**
  11th Position Worldwide

4. International Rover Challenge

The International Rover Challenge is an international competition organised by the Space Robotics Society. It challenges university students to conceptualise, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business planning and project management.

8th position worldwide (Debut Onsite Competition)

SMART INDIA HACKATHON 2024 - HARDWARE EDITION Winner–First Position

Team Name: ALT_24
Problem Statement: Target Detection by Optimizing Anomaly Detection in Hyperspectral Image Processing using AI/ML
PS ID: 1565
Team Members: Gargeya Parab, Isha Diwali, Isha Solanki, Soham Lotlikar, Suman Swain, Adit Shah
Mentors: Prof and Head of Department Dr Amit Deshmukh, Prof Tushar Sawant
About the competition: The Smart India Hackathon (SIH) 2024 provides a platform for students to tackle pressing societal and industrial challenges using innovative technological solutions. Our team, **ALT_24** from DJ Sanghvi College of Engineering, addressed PS ID: 1565, focusing on optimizing anomaly detection in hyperspectral image processing using AI/ML techniques. The proposed solution enhances anomaly detection capabilities for applications in defense, environmental monitoring, and resource management. By leveraging advanced machine learning algorithms, atmospheric correction methods, and cutting-edge denoising techniques, we aim to process hyperspectral data efficiently, detect anomalies accurately, and classify them effectively.
PS given by: National Technical Research Organization (NTRO)
Abstract: Hyperspectral imaging, with its ability to capture data across multiple wavelengths, holds immense potential for applications in defense, environmental monitoring, and resource management. However, accurate anomaly detection remains a significant challenge due to atmospheric distortions, noise, and computational inefficiencies.

Our solution leverages advanced AI/ML techniques integrated with robust pre-processing methods to detect and classify anomalies with precision. Key components include atmospheric correction using the 6S Radiative Transfer Model, denoising with a 3D Quasi-Recurrent Neural Network (QRNN3D), and anomaly detection using a Generative Adversarial Auto encoder (GAAE). These components are seamlessly integrated into a user-friendly web interface for hyperspectral image analysis and anomaly visualization.

This project achieves anomaly detection accuracy of 98.16% while reducing computational overheads through model optimization and GPU acceleration. By clustering anomalies using K-means and saliency mapping, we ensure efficient identification of critical regions within hyperspectral images. Our future plans include deploying real-time solutions on edge devices, developing open-source APIs, and creating cloud-based platforms for hyperspectral data processing.

With this project, we aim to transform hyperspectral imaging into a scalable and accessible technology, offering a robust framework for real-world applications.

Proposed Solution

Our solution integrates multiple AI/ML techniques to process hyperspectral images and detect anomalies. The framework includes:

1. **Atmospheric Correction**: Using the 6S Radiative Transfer Model, Dark Object Subtraction, and Flat Field Approach to correct distortions caused by atmospheric interference.
2. **Denoising**: Implementing a 3D Quasi-Recurrent Neural Network (QRNN3D) to remove noise and enhance image clarity while preserving spatial and spectral information.
3. **Anomaly Detection**: Utilizing Generative Adversarial Autoencoders (GAAEs) to detect and classify natural and man-made anomalies with an accuracy of 98.16%.

4. **Saliency Mapping**: Efficiently highlighting regions of interest using advanced mapping algorithms with computational time optimized to under 5 minutes.
5. **Web Interface**: An interactive platform that allows users to upload, process, and visualize hyperspectral images with anomaly detection outputs.

Key Features and Explanation

1. **Atmospheric Correction**
   - **Feature**: Corrects distortions in hyperspectral images caused by atmospheric scattering and absorption.
   - **Explanation**: The 6S model simulates atmospheric effects, while the Dark Object Subtraction and Flat Field methods adjust spectral radiance, ensuring accurate reflectance data for anomaly detection.
2. **Denoising with QRNN3D**
   - **Feature**: Removes various types of noise (Gaussian, sparse, mixed) while maintaining the integrity of the hyperspectral data.
   - **Explanation**: The QRNN3D architecture leverages spatial-spectral correlations with a quasi-recurrent pooling mechanism, enabling high-quality noise reduction in complex datasets.
3. **Anomaly Detection with GAAE**
   - **Feature**: Detects and classifies anomalies using a Generative Adversarial Autoencoder.
   - **Explanation**: The model combines encoder-decoder architecture, latent and reconstruction discriminators, and adversarial loss to achieve high accuracy and robustness in anomaly classification.
4. **Saliency Mapping**
   - **Feature**: Highlights potential anomalies for user review.
   - **Explanation**: By clustering anomalies and applying silhouette scoring, the system ensures rapid and precise identification of critical regions in the image.
5. **User-Friendly Web Interface**
   - **Feature**: Simplifies data upload, processing, and visualization for end-users.
   - **Explanation**: The web-based solution integrates AI/ML pipelines with an interactive dashboard, allowing seamless interaction for non-technical users.
6. **Optimization and Scalability**
   - **Feature**: Reduced computational times and adaptability to new datasets.
   - **Explanation**: Techniques like multithreading, model fine-tuning, and GPU acceleration ensure scalability and efficiency for real-time applications.

Conclusion

Our project demonstrates the potential of AI/ML in advancing hyperspectral anomaly detection, with significant implications for defense, environmental conservation, and resource management. The user-centric design and future plans for open-source API and cloud-based solutions aim to make hyperspectral data processing accessible and impactful for a wide range of applications.

Photographs:

Team DJS SURYA Shines Bright in Product Development Contest

In a remarkable achievement, Team **DJS SURYA** from **Dwarkadas J. Sanghvi College of Engineering** has secured the **1st position** in the **Design Phase of the Grand Challenge Contest 2024** on *Electronic Product Design & Development*.

The contest is organized by **Ministry of Electronics & Information Technology (MeitY), Government of India** and executed by **Centre for Development of Advanced Computing (CDAC), Noida** and the **India Cellular and Electronics Association (ICEA)**, was held under the prestigious project **"Establishment of Centre of Excellence (CoE) for Products Based on Li-ion Cells."**

Competition Details

The contest aims to foster innovation and excellence in Electronic Product Design. Teams across the nation participated, showcasing cutting-edge solutions to real-world challenges.

Problem Statement

The problem statement assigned to Team DJS SURYA, coded **P006**, was to design a **Portable Power Tank with Solar Charging**. Product supports diverse charging and discharge ports. This innovative product is tailored to address energy needs in off-grid, rural, and disaster-prone areas, combining renewable solar energy with advanced battery technology for reliable and sustainable power solutions.

Participants and Guidance

The winning team comprised the following members:

- **Chintan Limbad**
- **Darsh Kadecha**

The team was guided by **Dr. Amit Deshmukh and Prof. Pavan Borra**, whose expertise and mentorship played a pivotal role in this success.

Achievements

Team DJS SURYA's groundbreaking solution not only won accolades but also earned the following:

- **Prize Money**: INR 35,000 (5,000 tax deducted)
- **Product Development Fund**: INR 50,000

These funds will be instrumental in developing and refining the prototype and scaling it for real-world applications.

This achievement underscores the innovative potential of students at Dwarkadas J. Sanghvi College of Engineering and their commitment to tackling pressing global challenges. Team DJS SURYA has set a benchmark for excellence in electronic product design, inspiring peers and making the institution proud. Their work exemplifies how technological innovation can drive sustainable and impactful change.

Next phase of prototype demonstration scheduled in weeks ahead.

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY

ICEA INDIA CELLULAR & ELECTRONICS ASSOCIATION
Inspire.Enable.Lead

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING NOIDA

(A Scientific Society of Ministry of Electronics & IT, Government of India)

CERTIFICATE OF ACHIEVEMENT

No. CoE/GC-2024/DW/P-006

This certificate is awarded to ***Team DJS_SURYA*** for participating and securing the 1st Position in the Design Phase of Grand Challenge Contest 2024 on "Electronic Product Design & Development" for Problem Statement ***P006:To design a Portable Power Tank with Solar Charging***, conducted by CDAC, NOIDA and ICEA under the project "Establishment of Centre of Excellence (CoE) for Products Based on Li-ion Cells (Post-Cell)".

(Vivek Khaneja)
Executive Director
CDAC, Noida

(Sunita Verma)
Scientist-G and GC (R&D-E)
MeitY, New Delhi

(Rajesh Sharma)
Executive Director
ICEA, New Delhi

5 RESULT ANALYSIS

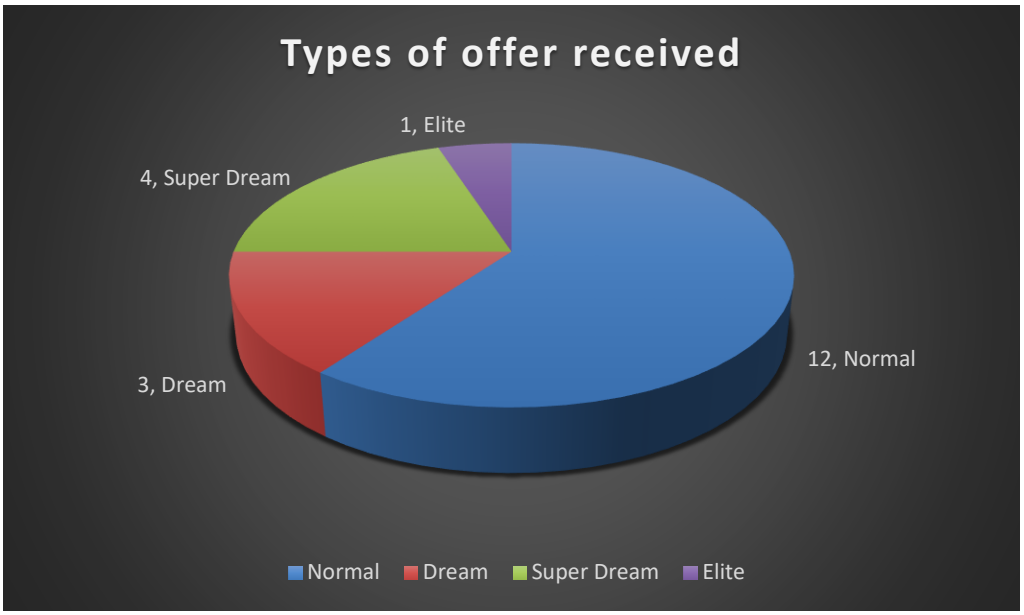
Academic Year : 2023-24

Sr. no.	Semester	Total no of students appeared	Total no of students passed	% of passing in the subject
1	III	204	185	90.69
2	IV	202	187	92.57
3	V	108	95	87.96
4	VI	108	103	95.37
5	VII	136	135	99.26
6	VIII	136	136	100

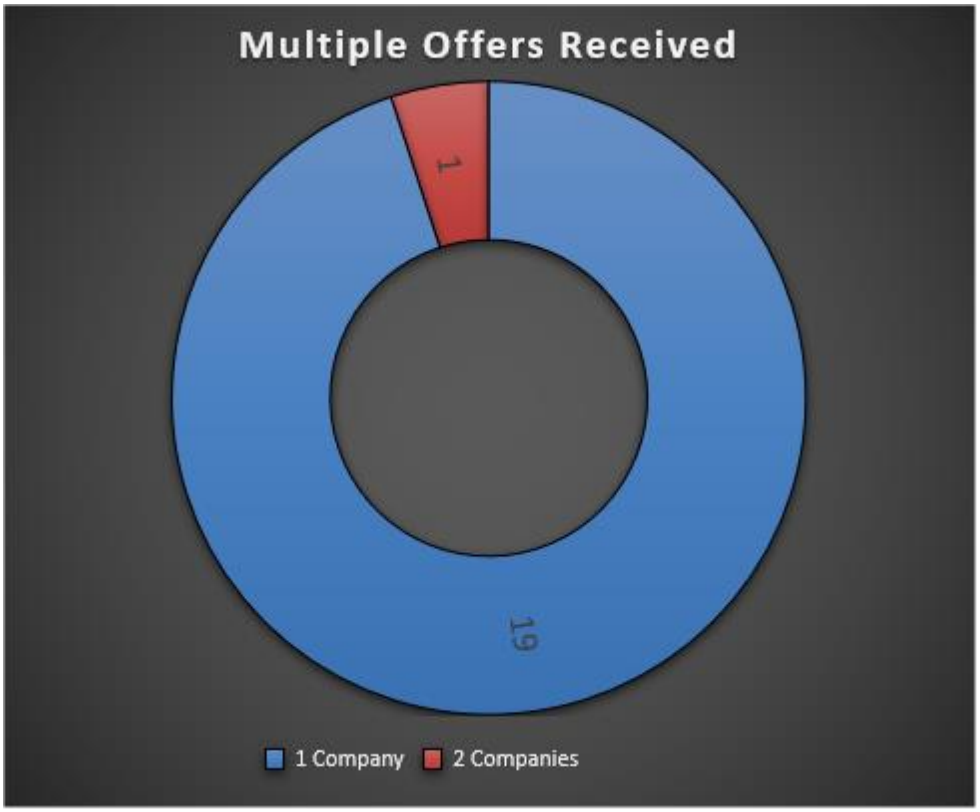
6 PLACEMENT DATA

Total no. of Students Placed Company Wise = 20 (Including Multiple Placement Offers)

Sr. No.	Company Name	Salary Per Annum(LPA)	No. of Students Placed
1.	Apollo	19.0	1
2.	UBS Bank	12.5	1
3.	Oracle	9.7	1
4.	Tresvista	8.4	2
5.	Frootle	6.1	3
6.	Capgemini	5.75 to 4.25	6
7.	TCS	3.3	6
Minimum CTC in LPA: 3.3 LPA		**Maximum CTC in LPA: 19.00 LPA**	



Ellite: >= 15 LPA, Super Dream: >8.0 LPA, Dream: 6.0 to 8.00, LPA, Normal: < 6.0 LPA


Multiple Offers Received
1
19
1 Company
2 Companies

Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

ACADEMIC BULLETIN

January 2025- May 2025

Department of Electronics & Telecommunication Engineering

Prepared by:

Prof. Supriya Dicholkar
(Assistant Professor, EXTC, DJSCE)

Prof. Amit A. Deshmukh
(Professor & Head EXTC, DJSCE)

ACADEMIC BULLETIN

Period: 1st January 2025 – 31st May 2025

Department of Electronics and Telecommunication

1. ABOUT DEPARTMENT

1.1 Department Information

- Started in the year 1999 with the intake of 30 and which was increased to 60 in the subsequentyear.
- The intake was increased to 120 in the Academic Year 2010 – 11.
- In the Academic Year 2011 – 12, Department has started M.E. Program in Electronics & telecommunication with an intake of 18 students.
- For the first time Department got NBA accreditation for two years from January 2013. In second Outcome based evaluation, Department got NBA accreditation for three years from July 2017.
- The Department started with Ph.D. program in Academic Year 2015 – 16 with an intake of 10 students.
- The department is having highly qualified, experienced and dedicated faculties and supportingstaff.
- Well-equipped labs and fully air-conditioned classrooms with projectors.
- The intake was increased to 180 in the Academic Year 2022 – 23.

1.2 Vision of the Department

To develop technically competent and socially responsible Electronics and Telecommunication engineers capable of fulfilling expectations at indigenous and global levels.

1.3 Mission of the Department

- To provide a conducive educational environment for students by providing goodinfrastructural facilities, knowledge base and excellent faculty support.
- To provide a strong foundation of core knowledge and exposure to research culture.
- To motivate learners to acquire adequate professional and soft skills, to develop personalitytraits and eventually transform them as life-long learners.
- To strive and achieve practical exposure by maintaining good rapport with industry and professional network.

1.4 Program Educational Objectives (PEOs)

- **PEO1:** To prepare learners for graduate studies by providing strong foundation of basic sciences, computer programing and thus, develop analytical aptitude, and problem-solving abilities.
- **PEO2:** To develop a fundamental understanding of electronic & integrated circuits, communication systems and allied disciplines.
- **PEO3:** To develop core competency and expertise in the diverse areas of communication covering Signal processing, Electromagnetic Engineering, Embedded Systems, ComputerCommunication and Advanced Wireless Networks domains.
- **PEO4:** To inculcate competencies and aptitude in extending acquired technical knowledge to solve real life issues with high professional and ethical standards.
- **PEO5:** To develop proficiency in soft skills and deliver adequate personality traits to enablethe pass outs to pursue higher education, to find competitive employment opportunities and/or pursue entrepreneurial ventures.

1.5 Program Specific Outcomes (PSOs)

- Design and implement electronic systems that perform analog and digital signal processing functions as applied in embedded systems, multimedia processing and VLSI design.
- Design and implement necessary components (circuits, antennas, microwave devices) of modern RF/Wired/Wireless communication systems.
- Cultivate necessary soft skills, aptitude and programming skills to solve real-world problems.

2. ADMINISTRATION

IETE COMMITTEE

Prof. Amit Deshmukh — Dr. Anuja Odhekar

PROJECT COORDINATOR

Prof. Amit Deshmukh — Dr. Ameya Kadam

DEPARTMENTAL LIBRARY

Prof. Amit Deshmukh — Prof. Archana Chaudhari

ALUMNI COMMITTEE

Prof. Amit Deshmukh — Prof. Ranjushree Pal

NBA CORE COMMITTEE

Prof. Amit Deshmukh — Dr. V. V. Kelkar (PC/NC)

Dr. Ameya Kadam — Dr. Venkata A. P. Chavali

AUTONOMY COMMITTEE

Dr. S. B. Deshmukh — Dr. Poonam Kadam

TIME-TABLE COMMITTEE

Dr. Venkata APC — Prof. Archana Chaudhary

PLACEMENT COORDINATOR

Dr. Aarti Ambekar

NPTEL and IBM COORDINATOR

Dr. V. V. Kelkar

Department of Electronics and Telecommunication

3. IETE- SF

The Electronics and Telecommunication Department of Dwarkadas. J. Sanghvi College of Engineering presents Institution of Electronics and Telecommunication Engineers- Student Forum (**IETE-SF**). The student chapter with a working force committee of 22, consisting of **second year** and third **year students**, hosted a few of the most quintessential and technically challenging events. A membership drive was conducted at the start of the year with an overwhelming response. (www.djsceietesf.com)

IETE Organizing Committee Structure

IETE SF Branch Counsellor: - Dr. Anuja Odhekar

Chairman	Utkarsh Lotiya
Vice-Chairperson (Admin)	Aneesh Joshi
Vice-Chairperson (Technical)	Samay Mehta
Secretary	Radhika Kadu
Treasurer	Gauransh Singh Bedi
DJ-Strike Co-ordinator	Harshil Khara Vaishnavi Pawar Manjiri Kale Shravanee Madhale

Head Of Departments:	
Publicity	Isha Solanki Vinil Shah
Marketing	Purav Ashar Nandini Mandekar
Technical	Sairudra Gudur
Infotech	Prashant Sherkar
Creatives	Nidhi Gandhi Parth Mehta
Events	Aditya Naik
Book Bank	Kartik Panchal
Component Bank	Kartik Panchal

3. DEPARTMENT ACTIVITIES

3.1 Value Added Program under IETE-SF

Book Bank

IETE-SF provides the students with a book bank facility where they can issue reference books at nominal rates for the entire semester. Students who want a better insight into the subject avail this facility as these reference books aid in developing a good understanding of the topics and enable them to consolidate their foundation of the subject. Book bank has more than 60 book titles as per the syllabus requirement for 3rd to 8th semester. This activity not only motivates students to use reference books prescribed in syllabus but also explore them in the library management system. The alumni who worked as "Book-Bank" coordinators received paid assistance-ship in the library during their master program.

Component Bank

IETE-SF provides a component bank facility where students can borrow electronic components which they require for executing multiple projects both in and outside of the curriculum. They can utilize the facility by initially paying 50% of the cost and getting a refund of 20% on returning the components, provided that they are undamaged.

3.2 Industrial visit at GMRT under IETE-SF

Date of the Event: 10th January 2025

Time: 9:30 AM – 5:30 PM

Participants: TE EXTC Students

Venue: GMRT Observatory, Khodad, Narayangaon

Objectives of the activity:

The industrial visit to the Giant Metrewave Radio Telescope (GMRT) Observatory, organized by the IETE Students' Forum of DJSCE, aimed to bridge the gap between academic knowledge and practical experience in the field of radio astronomy and large-scale instrumentation. It was an opportunity for students to explore one of the world's most advanced radio telescope arrays and understand the technologies that power deep space exploration.

CONTENTS:

On 10th January 2025, TE students of the Electronics and Telecommunication Department, accompanied by faculty, visited the Giant Metrewave Radio Telescope (GMRT), located in Khodad, Narayangaon. The GMRT is operated by the National Centre for Radio Astrophysics (NCRA) under the aegis of the Tata Institute of Fundamental Research (TIFR). Built between 1984 and 1996 under the vision of Dr. Govind Swarup, a pioneer in Indian radio astronomy, GMRT is globally renowned for its unmatched capabilities in observing celestial phenomena at low radio frequencies.

Located in a rural area to minimize radio frequency interference and atmospheric noise, the GMRT site houses 30 fully steerable parabolic dishes, each with a diameter of 45 meters. These are arranged in a distinctive Y-shaped configuration, spread over 25 km, a layout that ensures exceptional resolution and sensitivity while detecting faint cosmic signals.

The term Giant Metrewave Radio Telescope is a direct reflection of the facility's key characteristics. It is one of the world's largest and most powerful radio telescopes, specifically designed to observe signals in the metre-wavelength range, operating across frequencies from 50 MHz to 1500 MHz. These radio signals are emitted by celestial bodies and carry vital information about the nature of the universe.

During the visit, students explored the engineering marvels behind each component of the GMRT system. The parabolic dishes, constructed using mesh surfaces, reduce wind resistance while preserving the ability to reflect incoming radio waves toward the focal point. Each dish is mounted on a system that provides azimuthal rotation and elevation adjustment, enabling it to track cosmic sources with high precision. The quadripod support structure, with four robust steel legs, holds the turret/feed assembly precisely at the focal point. This feed assembly includes frontend boxes and a suite of filters—bandpass, notch, and low-noise amplifiers (LNAs)—to convert, clean, and amplify incoming signals while mitigating terrestrial interferences.

Currently, four frequency bands are actively used—150 MHz, 325 MHz, 610 MHz, and 1420 MHz—while Band 1 remains under testing. These signals are passed to a common box containing a band selector, which further channels the data down through two output channels.

A notable feature of the GMRT infrastructure is its counterweight system, used to balance the massive 80-tonne antenna structure. With an additional 40-tonne counterweight, the total assembly achieves

mechanical stability during rotation and movement. The base of each antenna is embedded into a reinforced concrete foundation to minimize vibration, while a central pedestal houses the azimuthal drive and control electronics.

The antenna movements are managed by precision motors, coordinated through a system of encoders and limit switches that prevent misalignment and ensure safe operation. The entire telescope array is remotely operable and highly synchronized, functioning as an interferometric array. This configuration allows all 30 dishes to operate in unison, combining signals for enhanced image reconstruction.

The facility is also equipped with safeguards such as wind-resistant structures, lightning arrestors, and solar attenuators to protect the antennas and electronics from environmental hazards. Signals from all dishes are transmitted to a central processing facility via high-speed optical fibre links, ensuring high data integrity over long distances.

At the heart of the GMRT's processing system lies the Correlator, which mathematically compares the signals from each pair of antennas to extract phase and amplitude differences. This forms the foundation for reconstructing high-resolution images and spectra of observed cosmic regions. The data undergoes extensive processing using Digital Signal Processing (DSP) techniques, including Fourier transformations, filtering, and noise removal. These processes are handled using high-speed processors and Field Programmable Gate Arrays (FPGAs).

In the server room, the operation of the GMRT is managed through four large racks housing critical systems for coordination, data processing, and network communication. The GMRT Time Allocation Committee (GTAC)determines observation schedules, ensuring optimal utilization of the telescope. The room is shielded to minimize Radio Frequency Interference (RFI) and is maintained under controlled conditions for performance and longevity.

The visit also provided insights into the software ecosystem used for telescope control and data analysis. The Telescope Control System (TCS) automates antenna alignment and observation tracking, while post-processing is carried out using powerful tools such as AIPS (Astronomical Image Processing System). The central clock, running at 800 MHz, ensures time-synchronization across the network.

Students were also introduced to the ongoing challenges faced by the GMRT, such as RFI suppression, signal integrity preservation, and the mitigation of astronomical and geographical errors. The team demonstrated how these challenges are overcome using algorithmic corrections and signal calibration techniques.

The GMRT has undergone several significant improvements in recent years. Its frequency range has expanded from a narrow 32 MHz to a wide 400 MHz, offering greater observational flexibility. Upgrades to the low-noise amplifiers and signal paths have greatly enhanced sensitivity, while the backend processing system has transitioned to FPGA and GPU-based architectures, increasing frequency resolution from 256 channels to 4000.

Photographs of the Event:

3.3 Seminar on Technical Paper under IETE-SF

Date of the Event: 7th February 2025

Time: 4.00 PM – 6.00 PM

Participants: TE EXTC Students

Speaker: Dr. Satishkumar Chavan

Objectives of the activity:

The primary objective of the *Technical Paper Seminar* was to equip students with the necessary knowledge and skills to undertake research-oriented writing, which is a critical component of both academic and professional growth. The seminar aimed to:

- Introduce students to the technical aspects of writing and publishing research papers.
- Familiarize students with Overleaf – a collaborative LaTeX editor used for professional document preparation.
- Explain the process of ensuring academic integrity through plagiarism detection and avoidance.
- Provide a structured approach on how to begin and develop a research paper from scratch.

CONTENTS:

The session commenced promptly at 4:00 PM with a welcome address, following which Dr. Satishkumar Chavan, an esteemed academician and subject expert, took over the session. The seminar was carefully structured to progress from basic concepts to more detailed strategies, ensuring that students of all experience levels could follow and benefit.

A. Introduction to Overleaf

Dr. Chavan began by introducing Overleaf, a powerful LaTeX-based platform widely used for writing technical and scientific documents. Key areas covered included:

- Navigating the Overleaf interface.
- Working with templates for IEEE and other publication standards.
- Incorporating references, citations, equations, figures, and tables.
- Collaborating with co-authors using Overleaf's real-time editing and commenting features.

This segment was accompanied by a live demonstration to help students visualize the application of concepts in real time.

B. Techniques of Technical Paper Writing

The seminar continued with an in-depth discussion on the methodology of writing a technical paper. The speaker emphasized the following components:

- Structuring a research paper – Title, Abstract, Keywords, Introduction, Methodology, Results, Discussion, Conclusion, and References.
- Writing with clarity, objectivity, and academic tone.
- The importance of literature review and how to critically analyze sources.
- Proper use of technical vocabulary and graphical illustrations to enhance comprehension and impact.

C. Plagiarism and Academic Integrity

One of the most crucial segments of the seminar addressed the ethical aspects of research writing. Students were educated on:

- What constitutes plagiarism – both intentional and unintentional.
- Tools and techniques to detect and prevent plagiarism.
- Citing sources correctly using citation styles (IEEE, APA, MLA, etc.).
- Consequences of academic misconduct in educational and professional settings.

Real-world examples and software tools such as Turnitin and Grammarly were referenced to demonstrate how plagiarism is detected.

D. Initiating a Research Paper

Finally, Dr. Chavan provided a step-by-step framework for starting a research paper, focusing on:

- Identifying a research gap.
- Formulating research questions and hypotheses.
- Planning experiments or simulations, data collection, and analysis.
- Drafting an initial outline and progressively refining it into a complete manuscript.

Photographs of the Event:

Impact and Learning Outcomes

The *Technical Paper Seminar* had a significant impact on the academic development of the students who attended. It provided them not only with practical skills but also with a deeper understanding of the research process and its ethical framework. The comprehensive nature of the session ensured that students left with a broader perspective and readiness to engage with scholarly activities. The key outcomes of the seminar are outlined below:

1. Enhanced Research Preparedness

The session served as a foundational platform for students who are new to the world of academic research. Through structured guidance on how to begin writing a research paper, the seminar demystified what can often be an intimidating process. Students were shown how to identify research gaps, pose relevant questions, and build a coherent framework for their papers. This has better equipped them to participate in university-level research projects, paper presentations, and technical competitions with confidence.

2. Improved Technical Documentation Skills

Exposure to **Overleaf**, an industry-standard LaTeX-based editor, enabled students to familiarize themselves with professional documentation tools used in journals and conferences worldwide. Understanding the format and structure of IEEE-style papers, and the correct incorporation of citations, figures, equations, and references, has given students the ability to present their research in a format acceptable by leading academic forums. This proficiency will serve them well throughout their academic and professional careers.

3. Increased Awareness of Ethical Research Practices

The seminar emphasized the importance of academic integrity, placing considerable focus on the issue of **plagiarism**. Many students were previously unaware of the subtleties and seriousness of plagiarism, including unintentional plagiarism that can occur through improper citation. Dr. Chavan's explanation of plagiarism detection tools, including a demonstration of how they function and interpret results, added practical value to this discussion. As a result, students left with a more ethical approach to research writing, understanding that originality and honesty are fundamental to scholarly work.

4. Greater Confidence in Academic Writing

For many students, the thought of writing and publishing a technical paper can be daunting. However, the seminar broke down the process into manageable steps, offering tips on everything from ideation and literature review to drafting and final editing. Real-world examples shared by the speaker helped students relate theoretical knowledge to actual practice. This has greatly improved their confidence and motivation to begin their own research papers or collaborate with faculty on ongoing projects.

5. Motivation Toward Research and Innovation

Beyond technical skills, the session served as an inspiration for students to view research not just as an academic requirement, but as a valuable process of inquiry, exploration, and contribution to their field. Several students expressed a renewed interest in exploring topics they were curious about, with a goal to potentially publish their work in academic journals or present at conferences.

6. Interdisciplinary Applicability

The concepts covered during the seminar were not limited to a single domain but were applicable across various branches of engineering and science. The versatility of Overleaf and LaTeX for thesis writing, technical reports, and collaborative research projects was discussed, making the session beneficial to students from multiple disciplines.

7. Long-term Academic and Professional Benefits

Mastering the skills shared in the seminar gives students a competitive edge in both higher education and industry. Universities and employers increasingly value individuals who have demonstrated the ability to write and publish technical papers. Participation in such seminars reflects a commitment to academic excellence and positions students as future contributors to research and development.

Feedback from Participants

The feedback collected from participants highlighted the relevance and practicality of the seminar. Many students expressed appreciation for the hands-on guidance and the clarity provided on previously ambiguous aspects of paper writing and plagiarism.

Conclusion

The *Technical Paper Seminar* served as a pivotal academic initiative aimed at bridging the gap between theoretical knowledge and practical application in research documentation. Under the guidance of Dr. Satishkumar Chavan, students were not only introduced to the mechanics of writing a technical paper but were also encouraged to uphold academic integrity and contribute meaningfully to the research community. The session concluded at **6:00 PM**, leaving the participants motivated and better prepared for their academic and professional pursuits.

3.4Alumni meet 2025 under IETE-SF

Date of the Event: 15th February 2025

Venue: Seminar Hall, Dwarkadas J. Sanghvi College of Engineering

Time: 10am – 3pm

Objectives of the activity:

- To strengthen the connection between current students and alumni through knowledge-sharing and mentorship.
- To provide students with insights into real-world career paths, industry expectations, and opportunities beyond academics.
- To showcase the diverse achievements of alumni and inspire students to carve their own unique journeys.
- To foster a sense of belonging, pride, and continuity within the DJSCE community through alumni engagement initiatives.

Contents:

On 15th February 2025, the Electronics and Telecommunication (EXTC) Department of Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized an Alumni Meet to reconnect with past students and provide a platform for meaningful interactions between alumni, faculty, and current students. The event aimed to strengthen the alumni network, facilitate knowledge-sharing, and offer valuable career insights to students.

Event Proceedings:

The event began with alumni registration, where attendees were welcomed and presented with diaries as mementos. Alumni joined both offline and online via Microsoft Teams, allowing a diverse group to participate. Alumni from the years 2008-2024 were all attending thus proving to be a varied group with different amount of work experience under their belts.

The offline alumni shared their experiences at Dwarkadas J. Sanghvi College of Engineering, their professional journeys, and insights into industry trends. This was followed by an interactive Q&A session, where students asked questions about career paths, skills, and industry expectations. Online attendees also actively participated, sharing their experiences and advice with the students.

Throughout the session, alumni had the opportunity to reconnect with faculty members and fellow alumni, discussing their professional growth and reflecting on their college experiences. The event concluded with lunch, providing a relaxed atmosphere for informal networking and strengthening bonds within the EXTC community.
The event was successfully hosted by Third Year Mentor Vinil Shah, along with Tanvi Mehta, Anmol Parikh, Tanvi Gupte, and Yusuf Khambaty (Second Year), who helped manage and coordinate the event.

Participant Feedback and Reflections

The alumni meet received positive feedback from both students and alumni. Students found the session insightful and motivating, gaining practical advice on career development and industry trends. Alumni, in turn, expressed their appreciation for the opportunity to reconnect with faculty and peers, emphasizing the importance of staying connected with their alma mater. Many alumni also expressed interest in mentoring students and participating in future department initiatives.

Photographs of the Event:




ACKNOWLEDGEMENTS:

The success of the EXTC Department Alumni Meet was made possible by the dedicated efforts of the faculty and organizing team. A special thank you to Prof. Ranjushree Pal (Alumni Coordinator) for her leadership in planning and executing the event, and to Dr. Amit Deshmukh, Head of the EXTC

Department, for his unwavering support and encouragement. We also extend our gratitude to all the alumni who took the time to attend and share their valuable experiences, both in person and online.

IMPACT:

The Alumni Meet 2025 was a memorable and enriching experience, reinforcing the strong relationship between past and present students. Events like these play a crucial role in fostering mentorship, collaboration, and lifelong connections within the EXTC community. The department looks forward to organizing more such meaningful interactions in the future, ensuring continuous engagement and learning for students and alumni alike.

This version correctly attributes the event to the EXTC Department Faculty while maintaining a professional and engaging tone. Let me know if you need any refinements!

3.5 UnPlugged 2.0: 24-Hour National Hardware Hackathon under IETE-SF

Date of the Event: 8th & 9th March 2025

No. of Participants: 250 UG Engineering Students

Duration: 24 Hr

Objectives of the activity:

The aim of the event was to foster innovation in hardware design by immersing students in problem-solving challenges that reflect the growing needs of modern urban environments. The hackathon served as a national-level platform where budding engineers could push the boundaries of their technical creativity and collaboratively engineer impactful solutions. Through this, the event sought to promote cross-disciplinary thinking, encourage system-level design, and enhance the hands-on capabilities of young innovators.

CONTENT:

The IETE Students' Forum at Dwarkadas J. Sanghvi College of Engineering, Mumbai, successfully hosted the second edition of its national 24-hour hardware hackathon, UnPlugged 2.0, on the 8th and 9th of March 2025. This event carried forward the legacy of its inaugural edition by once again bringing together talented student engineers from all across India to address the complex and pressing challenges of today's urban landscape. The theme for UnPlugged 2.0 was Smart City Infrastructure and Sustainability, a fitting foundation for the challenges that lay ahead for the participants.

The hackathon was divided into three distinct rounds, each with its own technical rigor and emphasis. **Round One** began prior to the event days and was designed as a proposal round. In this stage, participants were required to submit a PowerPoint presentation outlining their conceptual approach to a given problem statement. The challenge was to propose an integrated IoT hardware solution that could reimagine urban traffic management, environmental monitoring, and public safety in the context of a smart city. This round encouraged teams to think holistically and propose real-time monitoring and control frameworks that could eventually be translated into working prototypes.

Round Two took place during the hackathon and was a simulation-based round focusing on design tools. Participants were asked to simulate and develop a modular printed circuit board (PCB) for an advanced central monitoring system named the Smart City Environmental Sentinel. Using software tools such as KiCad and Fusion 360, the teams had to create a power-efficient and scalable design architecture capable of integrating sensor interfaces, power management, and real-time data transmission. The simulation process demanded high precision, not only in electronic layout design but also in the accompanying 3D CAD modeling. Participants had four hours to complete and submit their designs, adhering to strict constraints on connectivity and power consumption.

The final round marked the culmination of the hackathon and tested the participants' ability to implement a comprehensive solution integrating both hardware and software elements. With rapid urbanization posing new systemic challenges, teams were tasked with building an autonomous urban intelligence system that brought together IoT-driven monitoring, multi-sensor data fusion, and predictive AI models. The final prototype had to be fully functional and capable of real-time decision-making through edge AI technologies. The implementation also required integration with a web and mobile-

based dashboard for visualization, as well as a cloud-connected analytics pipeline. The complexity and scope of this round made it a true test of design thinking, systems engineering, and collaborative execution.

WINNERS AND PRIZES:

The hackathon concluded with the announcement of winners whose solutions stood out for their innovation, completeness, and real-world relevance. The winning team, MangoDB from Pillai College of Engineering, Navi Mumbai, secured the top spot and was awarded a cash prize of ₹50,000. The first runner-up was Team LED from Hindustan Institute of Technology and Science, Kelambakkam, Tamil Nadu, who received ₹30,000. The second runner-up, Eco-Wolves from Shri Eshwar College of Engineering, Tamil Nadu, won ₹20,000 for their commendable efforts.

Photographs of the Event:

IMPACT:

- UnPlugged 2.0 created a lasting impression on all who participated. The event offered a unique blend of theory, simulation, and hands-on building, pushing students beyond conventional classroom learning. Participants engaged in intensive design thinking, multitasking under pressure, and full-stack engineering—from sensors and circuits to cloud and AI integration. The hackathon successfully bridged the gap between hardware and software disciplines and demonstrated the practical value of interdisciplinary knowledge. Moreover, it offered an opportunity for peer learning, mentorship, and exposure to real-world problem solving—critical skills for the engineers of tomorrow. The national-level nature of the event also allowed for the exchange of ideas across regions and institutions, making the experience both competitive and collaborative.

- UnPlugged 2.0 marked a significant milestone in the IETE-ISF journey of encouraging hardware-based innovation. The hackathon was not merely a competition but a platform for building the future—one prototype at a time. By successfully blending imagination with implementation, the event exemplified the power of student-driven technology in tackling urban challenges. With its tremendous success, UnPlugged 2.0 has set the bar high for future editions and reaffirmed the role of engineering students in shaping tomorrow's smarter, more sustainable cities.

3.6 Seminar on Optical Communication under IETE-SF

Date of the Event: 9th April 2025

No. of Participants: 80 TE BE students

Speaker: Mr. Kartik Parikh, CEO of Fastech Telecommunications

Time: 10.30 am – 12.30 pm

Objectives of the activity:

- To familiarize students with the concepts, technologies, and real-world applications of optical communication in the context of 5G and beyond.
- To provide industry-level insights into how telecom companies are adopting optical networks to meet growing data and connectivity demands.

CONTENT:

As we stand on the threshold of a hyper-connected future powered by 5G and beyond, the Department of Electronics and Telecommunication Engineering, in association with IETE-ISF, organized a highly insightful seminar titled *"Optical Networks: For 5G Communication and Beyond"* on April 9, 2025. The event witnessed enthusiastic participation from both Third Year and Final Year EXTC students. The session was conducted from 10:30 AM to 12:00 PM, offering a compelling look into one of the most critical technologies shaping modern communication.

The seminar was graced by Mr. Kartik Parikh, the CEO of Fastech Telecommunications, a distinguished leader with over 30 years of experience in the telecom industry. Under his guidance, Fastech has played a significant role in supplying advanced telecom testing and networking solutions to leading service providers across India. Mr. Parikh's expertise and practical knowledge brought immense value to the session, offering students a rare glimpse into real-world industry applications of optical networking.

The session began with a formal welcome, followed by Mr. Parikh's address, where he elaborated on the evolution of communication networks — from copper cables and coaxial systems to the highly efficient, high-capacity fiber-optic networks that form the backbone of today's telecom infrastructure. He highlighted how optical communication is essential for meeting the ultra-high data demands of emerging technologies, including 5G, the Internet of Things (IoT), AI-driven services, autonomous vehicles, and smart infrastructure.

Mr. Parikh took a deep dive into the fundamental principles of optical communication, such as the transmission of information using light, the role of optical fibers in minimizing loss and latency, and how light signals are converted, modulated, and multiplexed to carry vast volumes of data across continents. He explained how Wavelength Division Multiplexing (WDM) and Dense WDM (DWDM) have revolutionized data transmission by allowing multiple light signals to be carried simultaneously on a single fiber strand.

The audience was particularly engaged when Mr. Parikh shared real-life case studies of how companies such as Jio and Airtel have transitioned to fiber-to-the-home (FTTH) models, introducing services like Jio AirFiber to ensure last-mile connectivity at blazing fast speeds. He explained how such innovations

are enabling not only high-speed broadband but also low-latency applications like remote surgery, smart factories, online gaming, and real-time surveillance.

He also touched upon the challenges faced in optical network deployment, including signal degradation, installation complexities, maintenance of fiber lines, and the increasing need for automated network management systems. The talk covered how next-gen networks will incorporate software-defined networking (SDN) and network function virtualization (NFV) to enhance flexibility and responsiveness in service delivery.

The session concluded with a highly interactive Q&A segment, where students raised thoughtful queries about topics ranging from the future of satellite-based internet, integration of optical networks with wireless systems, to the skills required to build a career in optical and telecom sectors. Mr. Parikh answered every question with practical insights and encouraged students to continuously upskill and explore interdisciplinary learning — combining knowledge of optical physics, electronics, and software engineering.

The seminar proved to be immensely beneficial in expanding the students' understanding of the critical infrastructure behind global connectivity, and its role in shaping the next decade of technological advancement. With practical applications, technical depth, and an industry-oriented perspective, this session left a lasting impact on all attendees.

Photographs of the Event:

IMPACT:

1. **Technical Enrichment:** The seminar provided students with in-depth exposure to the architecture and functioning of optical networks, significantly enhancing their technical understanding of modern communication systems. Concepts such as fiber optics, WDM, and network virtualization were explored, equipping attendees with foundational knowledge essential in today's telecom landscape.
2. **Academic Empowerment:** By bridging the gap between classroom theory and industry application, the seminar deepened students' grasp of core communication subjects. Learning about cutting-edge technologies like 5G, AirFiber, and smart infrastructure deployments empowered students to approach academic projects and research with a more practical and future-oriented mindset.
3. **Career Awareness and Industry Insight:** The interaction with an industry stalwart like Mr. Kartik Parikh gave students firsthand insight into real-world telecom challenges and career opportunities. Understanding how major service providers adopt optical technologies to meet evolving demands opened up a clearer vision of the roles and skills expected in the telecommunications sector.
4. **Inspiration for Innovation:** The seminar served as a catalyst for innovative thinking by introducing students to the emerging applications of optical networks in IoT, AI, automation, and next-gen communication. Attendees left with a greater curiosity and motivation to explore interdisciplinary solutions and contribute meaningfully to ongoing tech revolutions.
5. **Knowledge Transfer and Collaborative Learning:** The session fostered an environment of active learning and engagement, particularly during the interactive Q&A. This encouraged the exchange of ideas not only between speaker and students but also among peers. As students internalize and share this knowledge, a ripple effect of learning is sparked, enriching the collective academic culture.

3.7 DJS WAVES: Parent body to DJS STRIKE and DJS SPARK under IETE-SF

Date of the Event: 11th April 2025

Time: 9:30 AM – 5:30 PM

No. of Participants: 250+ UG Engineering Students for both the competitions

Venue: Seminar Hall, Dwarkadas J. Sanghvi College of Engineering

Objectives of the activity:

- To provide a competitive yet inspiring platform for students to showcase hardware and tech-based innovations.
- To cultivate a spirit of practical engineering and idea validation through real-time demonstration and expert evaluation.
- To encourage interdisciplinary approaches and industry-ready thinking among budding engineers.

CONTENT:

DJS WAVES is the flagship event organized by IETE-ISF, DJSCE, serving as the parent body to two major competitions—DJS STRIKE and DJS SPARK. The event aims to bridge the gap between student innovation and industry insight by encouraging the development of purposeful, application-driven projects.

DJS STRIKE is the department-level project competition in which students from DJSCE presented their technical solutions and innovations. It focuses on encouraging in-house talent to tackle engineering challenges with creativity and rigor.

DJS SPARK, on the other hand, is a national-level project competition that welcomed participation from across the country. Conducted in a hybrid mode (online and offline), SPARK provided a national platform for student innovators to exhibit their hardware and software prototypes with real-world relevance.

The event began with an inaugural ceremony graced by the SPARK Judges:

- Dr. Savanna Bhise – Hon. Secretary, IETE Mumbai Centre
- Dr. Santosh Chapeneri – Lead Data Scientist, Wolters Kluwer

The STRIKE Judges panel included:

- Mr. Mayur Kulkarni – DJSCE & IIT Kharagpur alumnus; Strategy at Bristlecone
- Mr. Neeraj Gangrade – Founder, Ecosys Efficiencies Pvt. Ltd.
- Mr. Mrudul Parikh – Deputy GM, Corporate Strategy at Nayara Energy
- Mr. Nisarg Shah – GM, Reliance Jio; expert in AI/ML and green tech

A special moment during the ceremony was the unveiling of **'DJS Ignite'**, the official newsletter of IETE-ISF, unveiled by the Principal, Vice Principal, HOD, and the judges.
The competitions ran in parallel, with students from DJSCE and beyond presenting impactful ideas and solutions, judged on innovation, execution, and societal impact.

WINNERS AND PRIZES:

DJS STRIKE (Department-level project competition for DJSCE students):

- 2nd Runner-up: An IoT-based Battery Monitoring System for Backup Battery Storage
- 1st Runner-up: Real-time IoT and GIS-based Urban Management System
- Winner: Waste Management System

(Awards presented by the DJS STRIKE judges)

DJS SPARK (National-level hybrid project competition)

- 2nd Runner-up: An IoT-based Battery Monitoring System for Backup Battery Storage
- 1st Runner-up: Real-time IoT and GIS-based Urban Management System
- Winner: Waste Management System

(Awards presented by Prof. Amit Deshmukh, HoD, EXTC)

Photographs of the Event:

IMPACT:

DJS WAVES not only highlighted the technical brilliance of the students but also brought together minds from across the country to ideate and innovate. With expert mentorship, real-time demonstrations, and valuable industry exposure, the event left a lasting impact on all participants. It served as a reminder that student-driven innovation can be both transformative and solution-oriented.

3.8 Board of Studies Meeting

The Board of Studies meeting of Department of Electronics and Telecommunication Engineering was conducted in a hybrid mode on Saturday, 29th April, 2025 at 2 pm onwards in the conference room,

DJSCE. The meeting was held to discuss and approve:

1. Minutes of the meeting of 9th BOS meeting for approval.
2. Detailed scheme of semester Ill to semester VIll of DJS23 for discussion and approval.
3. Detailed syllabus of semester V& Vl ofDJS23 scheme and Honors program of DJS23 scheme.
4. Department PEO and PSO for approval.
5. Examiner panel of all the examinations to be conducted from July 2025 onwards for various subjects under DJ 19, DJS22 and DJS23 scheme.
6. Examiner panel for M. Tech examinations to be conducted from July 2025 onwards for DJS24 scheme.

The meeting was attended by the BOS members Dr. K. P. Ray, Dr. S. S. Mande, Dr. Sunil Kopparapu. Dr. Jayakrishnan Nir, Mr. Sumit Ranka BOS members and faculty members of the EXTC Department.

Following were the points discussed and the suggestions provided:

(i) Minutes of meeting of 9th BOS meeting were approved.

(ii) The UG DJS23 detailed syllabus for semester V& VI and Honors/Minor Degree Program Semester V subjects were presented for the approval. The suggestions made in the proposed svllabus of DJS23 curriculum are as follows:

a) Dr. Jaykrishnan Nair suggested to use GNU Radio for implementation of experiments in Analog and Digital Communication Laboratory Semester V course of DJS23.

b) Dr. K. P. Ray recommended to add "Book by Richard" for Radar Engineering Semester V course of DJS23.

c) It was suggested by Dr. Sudhakar Mande to include case studies related to Communication Engineering in Control System Semester V.

d) Dr. Sudhakar Mande suggested to remove resistive load inverter analysis in Digital VLSI course. Also he advised to include power analysis of CMOS inverter circuit.

e) Suggestion was made by Dr. Sunil Kopparapu to add TSMV for data visualization in honors program course Artificial Intelligence & Machine Learning. Also, to include latest edition of books and some online resources for reference.

f) For honors program course Intelligent loT, the name of the subject is not in line with the content of the subject. Hence it was suggested by Dr. Sunil Kopparapu to rename the subject accordingly. g) Dr. Sunil Kopparapu suggested to incorporate camera calibration in module I of Image Processing Course of Semester VI. Also, DFT can be removed.

h) Dr. Sunil Kopparapu suggested that in Data Compression and Encryption to include OGG format for audio signal.

i) Dr. Sunil Kopparapu suggested to redistribute the hours as per the content coverage in AIML course in semester VI.

j) Dr. Sunil Kopparapu also recommended to formulate the process in general for the cutting edge technology based courses to decide upon which books to be included as text books and reference books.

(iii) Suggestion was made by Dr. Sunil Kopparapu to replace the word "passout" by "graduate" in the PEOS statement of EXTC department.

(iii) Examiner panel for DJS22 & DJS23 UG curriculum and PG program was presented and approved by the committee.

Prof. Sheeja Nair Autonomy Coordinator EXTC Dept., DJSCE	Dr. Poonam A. Kadam Autonomy Coordinator EXTC Dept., DJSCE	Prof. Amit A. Deshmukh Professor & Head EXTC Dept., DJSCE

4. ACHIEVEMENTS

4.1 Faculty Publications- Conferences / Journals

Journal publication

Sr.No	First Author	Paper Details	Indexed by
1	Dr. Aarti G. Ambekar	Ambekar, A. and Deshmukh, A. (2025), Thinner Substrate Reconfigurable Design of Corner Truncated Square Microstrip Antenna for Polarization Agile Response in GSM Application. Int J Commun Syst, 38: e6119. https://doi.org/10.1002/dac.6119	SCOPUS
2	Dr. Satishkumar Chavan	Guruswamy S, Sharma B, Sable N, Chavan S. Prognosis of ovarian cancer multi-level-type for given cohorts to recommend the likelihood of treatment outcome. *Intelligent Decision Technologies*. 2025;0(0). doi:10.1177/18724981251325118	SCOPUS

4.2. Interaction of faculty with outside world

FDP/ STTP/Webinar/Workshop attended by Faculty Members:

Sr. No.	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Prasad S Joshi Dr. Satishkumar Chavan Dr. Vishakha Kelkar Dr. Anuja A Odhekar Dr. Sanjay Deshmukh Prof. Mrunalini Pimpale Dr. Aarti G. Ambekar Prof. Tanaji D. Biradar Prof. Yukti Bandi Prof. Sejal A. Kadam Prof. Abhilasha Raghtate Prof. Vivek Vijay Nar Prof. Ranjushree Pal Prof. Supriya Dicholkar Prof. Dipti Kale	ATAL FDP on "Cross Roads of AI and Signal Processing" at DJSCE	27th January to 1st February 2025

	Prof. Revathi A S Prof. Bahar C. Soparkar Prof. Renia Dias		
2	Prof. Mrunalini Pimpale Prof. Yukti Bandi	10 days FDP on "IoT and Machine Learning for Advanced Biomedical Signal Processing" at ABV-IIITM Gwalior	15th January to 24th January 2025
3	Prof. Tanaji D. Biradar Prof. Abhilasha Raghtate	ATAL FDP on "Quantum Computing: India's Journey Towards Quantum Excellence" at DJSCE.	13th January to 18th January 2025
4	Prof. Abhilasha Raghtate	AICTE Training And Learning (ATAL) Academy Faculty Development Program on Research and Innovation Trends in Large Language Models at Dwarkadas j Sanghvi College of Engineering (CSEDS)	20th January to 25th January 2025
5	Prof. Supriya Dicholkar Prof. Abhilasha Raghtate Dr. Satishkumar Chavan	One-week ISTE Approved Short Term Training Program (STTP) on "From Draft to Publication: Essential Steps in Research Article Writing"	6th January to 10th January 2025
6	Dr. Aarti G. Ambekar	Attended a one day seminar on "The Evolution of Power Management ICs in Semiconductor Industry" by by Prof. Qadeer Khan organized by IEEE-IISc VLSI Chapter.	5th January 2025
7	Prof. Supriya Dicholkar Prof. Dipti Kale	Attended a ATAL FDP on IoT integration with embedded systems	6th January to 10th January 2025
8	Prof. Ranjushree Pal	Attended a Atal FDP on The Role of Artificial Intelligence in Sustainable Waste Management.	10th February to 15th February 2025
9	Prof. Bahar Chetan Soparkar	Attended a ATAL FDP on Innovative Design Thinking Strategies for Next Generation AI Solutions	3rd February to 8th February 2025
10	Dr. Aarti G. Ambekar	Attended a webinar on "AI Accelerators: Reliability and Security Perspectives" by Prof. Biresh Joardar organized by IEEE-IISc VLSI Chapter.	5th March, 2025
11	Dr. Aarti G. Ambekar	Attended a webinar on "Deep Learning Computation and its Application" by Prof. Seok-Bum Ko organized by IEEE-IISc VLSI Chapter.	8th March, 2025
12	Dr. Anuja A Odhekar	Attended Intellectual Property Utsav	21st April to 26th April 2025
13	Prof. Dipti Kale	One-week ISTE Approved Short Term Training Program (STTP) on "From Draft to Publication: Essential Steps in Research Article Writing"	6th January to 10th January 2025

14	Prof. Abhilasha Raghtate	Completed ATAL FDP on "AI driven growth: shaping India's Economy and global leadership" at RGIT	24th February to 1st April 2025
15	Dr. Anuja A Odhekar	Completed 16 SESSIONS TRAINING ON INNOVATION AMBASSADOR	`13th February 2025
16	Dr. Poonam Kadam	completed this 40-hour (3-Credits equivalent) online training Program cum FDP on Foundations of VLSI Design Verification by MeitY and endorsed by AICTE/UGC.	23rd June to 5th July 2025
		Completed Innovation Ambassador(IA) training "Foundation Level" 30 hours.	2024-25

4.3. NPTEL/COURSERA Courses completed by faculty members:

Sr.No	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Satishkumar Chavan	NPTEL -12 week -"Computer Vision and Image Processing "	Jan-Apr 2025
2	Yukti Bandi	NPTEL+ Workshop Certificate on Signal Classification using Deep Learning	January 2025.
3	Supriya Dicholkar.	NPTEL -8 week ELITE + GOLD in -" Educational Technology and ICT"	Jan-Apr 2025
4	Dr. Ankita Malhotra	NPTEL -8 week -" Educational Technology and ICT"	Jan-Apr 2025
5	Abhilasha Raghtate	NPTEL -12 week -"Machine Learning for Engineering and Science applications "	Jan-Apr 2025
		Completed COURSERA COURSE ON AI FOR EVERYONE	19th June 2025
		Completed COURSERA COURSE ON FOUNDATIONS OF CYBER SECURITY	25th June 2025
6	Prof. Bahar Chetan Soparkar	NPTEL -8 week -" DESIGN THINKING FOR EDUCATORS"	JAN-MAY 2025
7	Dr. Poonam Kadam	NPTEL -12 week -" Design and Analysis of VLSI Subsystems "	Jan-Apr 2025

4.4. Faculty Achievements

Name of Faculty	Event description	Date
Prof. Amit A Deshmukh, Dr. Venkata A P Chavali, Dr. Aarti Ambekar, Prof. Tushar Sawant	Granted patent on with title Reconfigurable Sectoral Microstrip Antennas for wideband and circularly polarized response	30th June 2025
Dr. Prasad S. Joshi	Worked as Session Chair - MULTICON 2025, organised by TCET, Kandivali	21st February 2025
	Appointed as AICTE-IDEA Labs - Faculty Co-ordinator and received grant of Institute contribution 30L + AICTE, 30L + Industry / Alumni, 30L = 90L.	10th February 2025
Dr. Satishkumar Chavan	Worked as reviewer for 7th International Conference on Advances in Science and Technology, (ICAST 2025) organized by K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai and for Journal ACM Transactions on Multimedia Computing Communications and Applications.	April 2025
Dr. Vishakha Kelkar	got recognition as Active SPOC certificate from NPTEL	Jan-April 25.
Prof. Vivek Vijay Nar	Conducted one day hands-on workshop on 'Robotics and automation: Applications in Electrical Engineering' at SBMP	15th January 2025
Dr. Aarti G Ambekar	Recognized as a peer reviewer for the International Journal 1. IEEE Access and 2. International Journal of Communications Systems by Wiley	January, February 2025
	Recognized as a peer reviewer for 1. International Journal IEEE Access 2. International Journal Computing and AI connect.	March, 2025
Prof. Yukti Bandi Dr. Sunil Karamchandani Prof. Amit A. Deshmukh	granted design registration based on Smart Pest Control and Irrigation System.	9th April 2025
Prof. Supriya Dicholkar	Worked as reviewer for International Conference on Science Technology Engineering & Mathematics for Sustainable Development (ICSTEMSD-2025) and Worked as reviewer for 5th International Conference on Electrical, Computer and Energy Technologies, Paris , France.	February 2025
Prof. Abhilasha G. Raghtate	Worked as reviewer for Second International Conference on Electronics, Computing, Communication & Control Technology- 2025,ICECCC-2025, CMR Institute of Technology Bengaluru	February 2025

4.5.Student's participation in various events

DJS ANTARIKSH Team achievements

DJS Antariksh is the official Martian Rover Team of Dwarkadas J. Sanghvi College of Engineering, Mumbai, India established in 2019-20. The team consists of 50 passionate 2nd and 3rd year undergraduate students from diverse engineering disciplines who are united by a shared mission to push the boundaries of space exploration through innovation. The team's motto, 'To Decipher Unimaginable', embodies its commitment to space exploration. The team aims to represent India at various international competitions like the European Rover Challenge and International Rover Challenge, showcasing its commitment to advancing space exploration by developing cutting-edge autonomous Martian rover technology.

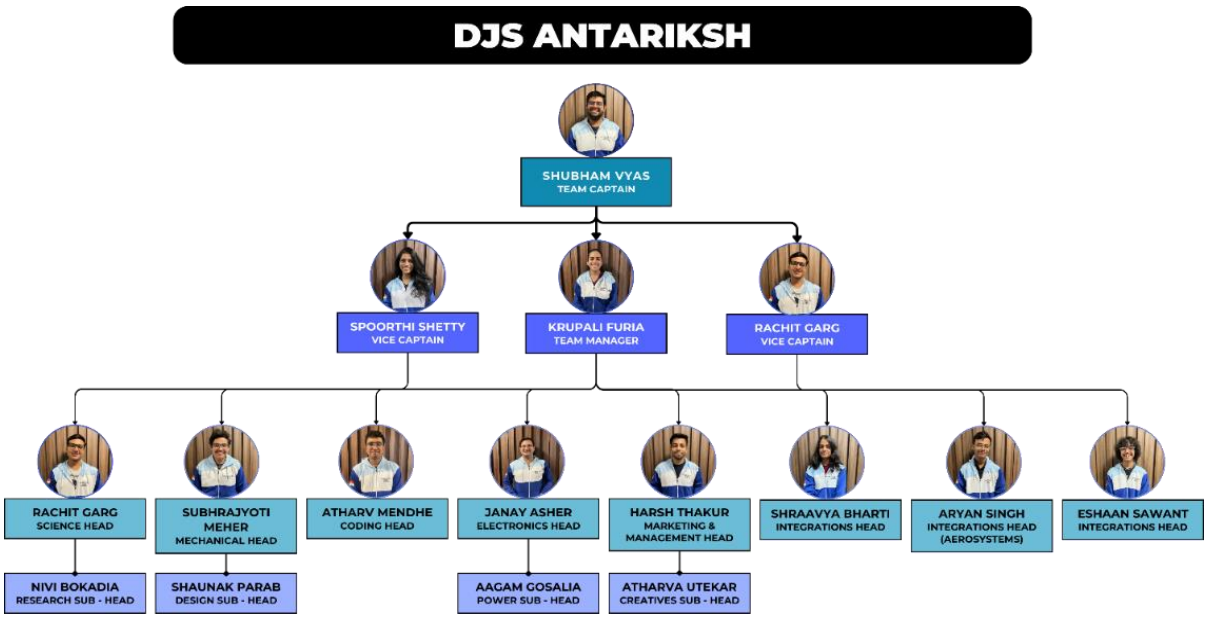
The team comprises of five departments: Electronics, Mechanical, Coding, Science, and Marketing, each contributing significantly to both technical and non-technical aspects of its operations. The team comprises of members with expertise across a broad spectrum of fields, including but not limited to Robotics, PCB and Circuit Design, Artificial Intelligence (AI) and Machine Learning, Additive Manufacturing and 3-D Design.

Team's Creations

ABHYAAN
(Team's Rover for ERC 2023 and IRC 2024)

PRAYAAN
(Team's Rover for IRC 2023)

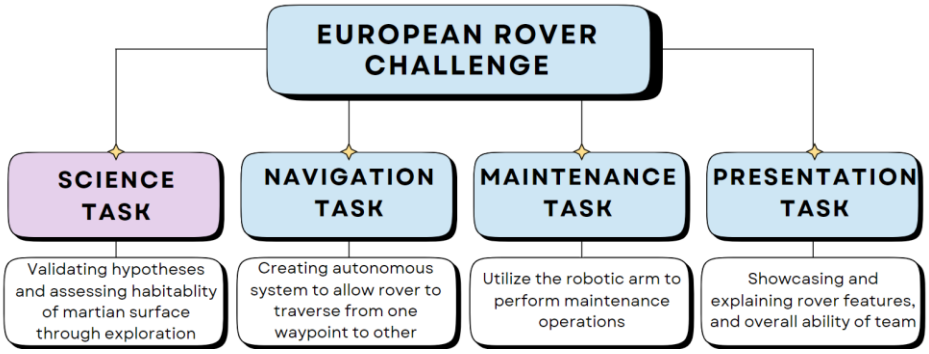
Team Structure (A.Y. 2024-25)



Competitions

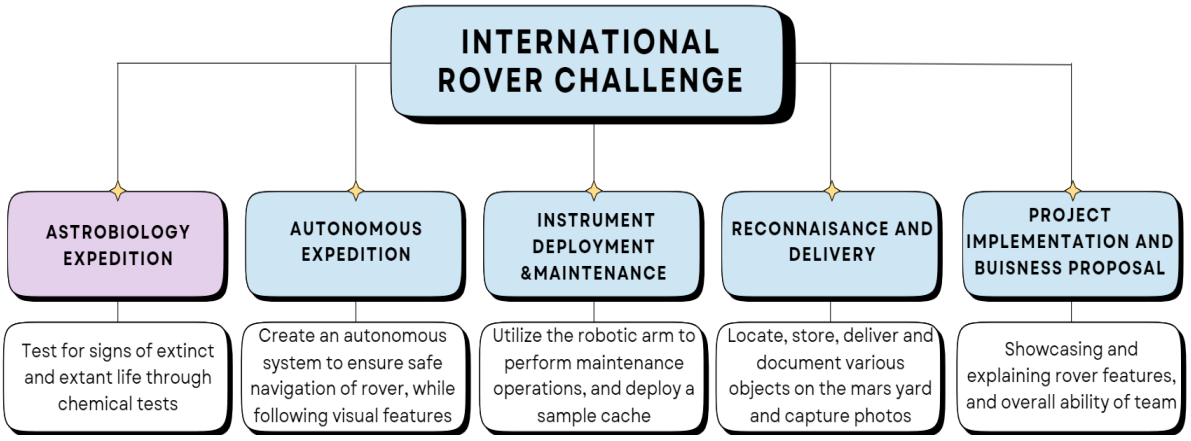
5. European Rover Challenge

The European Rover Challenge organised by the European Space Foundation takes place every year in Poland. It is an integrated programme working towards technological developments, specifically those in GPS-denied environments, with space exploration and utilisation as the leading theme. The ultimate goal of the ERC is to become a standardised test trial and benchmark for planetary robotic activities, coupled with strong professional career development platform. The competition is divided into 2 formulas: On-site and Remote.



6. International Rover Challenge

The International Rover Challenge is an international competition organised by the Space Robotics Society. It challenges university students to conceptualise, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business planning and project management.



7. International Rover Design Challenge

Space Robotics Society

International Rover Design Challenge (IRDC) is an online space engineering design and research competition by Space Robotics Society. It challenges university students to conceptualize and design Next-Gen Mars Rovers, which shall be fully equipped and mission ready for future astronaut-assistive exploration operations on Mars. Teams are supposed to carefully plan each sub-system of the Rover considering various extra-terrestrial parameters in design. This online research-oriented competition is designed for students to explore their mind and spark the innovative design thinking of individuals, free from constraints on available physical resources

8. International Rover Challenge

The International Rover Challenge is an international competition organized by the Space Robotics Society. It challenges university students to conceptualize, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business **planning and project management.**

Team's Achievement 2025

- **International Rover challenge 2025**

3rd position worldwide

- **International Space Drone Challenge 2025**

10th Position worldwide

- **European Rover Challenge 2025**

Qualified for on-site finals -Currently standing at 1st position worldwide

- **Featured in the Corporate Brief Section of the Indian Express and The Financial Express**

UPDATE (D. J. SANGHVI COLLEGE)

Dwarkadas J. Sanghvi College of Engineering, Mumbai securing 2nd Runner-Up position at the International Rover Challenge (IRC) 2025

DJS Antariksh, the official Martian Rover Team of Dwarkadas J. Sanghvi College of Engineering, Mumbai, has once again demonstrated its excellence on the global stage by securing the prestigious 2nd Runner-Up position at the International Rover Challenge (IRC) 2025. The competition, organized by the Space Robotics Society (SPROS), took place from 28th January to 2nd February 2025 at the BITS Pilani K K Birla Goa Campus. This marks the second consecutive year that DJS Antariksh has made it to the podium at IRC, having also secured the 2nd Runner-Up position in the 2024 edition. Their consistent top-tier performance underscores their commitment to excellence in space robotics. The team competed among the top 25 international teams that qualified for the finals, showcasing their technical prowess and problem-solving skills on a global stage. The International Rover Challenge is one of the most competitive space robotics contests, bringing together the brightest minds from around the world to design, build, and operate advanced planetary rovers capable of performing intricate tasks in simulated extraterrestrial environments. Expressing their excitement, the team stated, "Our journey at IRC 2025 has been a testament to months of relentless effort, rigorous testing, and an unwavering passion for space robotics. Securing the 2nd Runner-Up position on an international platform is a proud moment for us, and we are grateful for the support of our mentors, sponsors, and institution. With their motto, "ToDecipherUnimaginable", DJS Antariksh remains committed to shaping the future of planetary exploration through ingenuity, teamwork, and cutting-edge research.

5 RESULT ANALYSIS

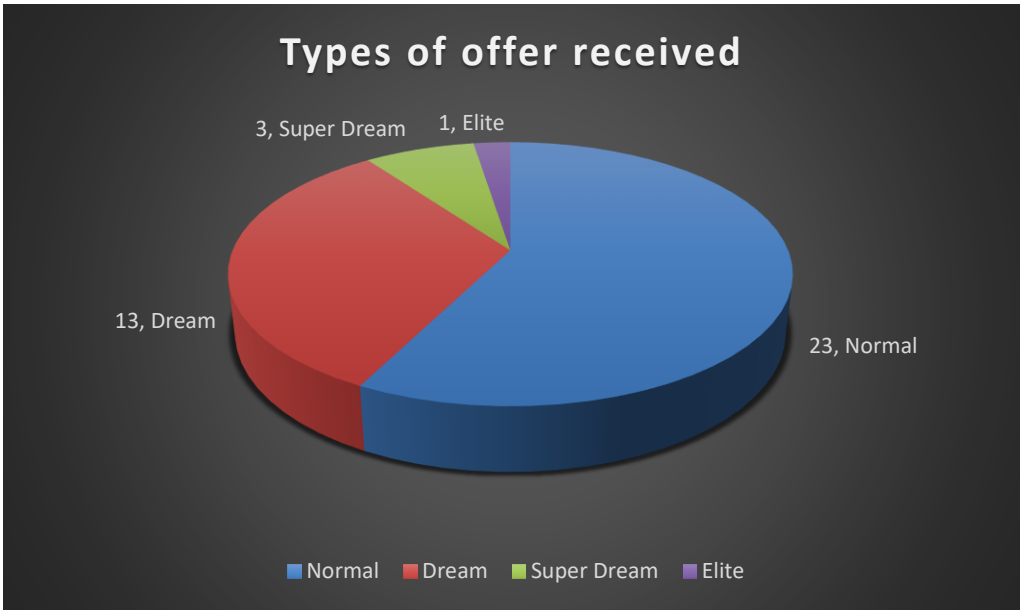
Academic Year : 2024-25

Sr. no.	Semester	Total no of students appeared	Total no of students passed	% of passing in the subject
1	III	203	193	95.07
2	V	206	198	96.12
3	VII	100	100	100

6 PLACEMENT DATA

7 Total no. of Students Placed Company Wise = 40 (Including Multiple Placement Offers)

Sr. No.	Company Name	Salary Per Annum(LPA)	No. of Students Placed
1.	Apollo	19.0	1
2.	UBS Bank	12.5	1
3.	Oracle	9.7	1
4.	Kishht	8-10	1
5.	Tresvista	8.4	2
6.	Montran	8.0	1
7.	Godrej	7.75	1
8.	Zeus Learning	7.05	1
9.	Cognitus	7.0	1
10.	Aurion Pro	7.0	1
11	EY	6.48	2
12.	Frootle	6.1	3
13.	Capgemini	5.75 to 4.25	6
14.	LogIQids	5.4	3
15.	Oberoi Realty Ltd.	5.0	1
16.	AGR	4.9	1
17.	Gandhi Automation	4.5	1
18.	Safran	4.5	1
19.	Concast	4.45	1
20.	Cognizant (Genc)	4.0	1
21.	L&T Technology Services	4.0	2
22.	Dhan	4.0	1
23	TCS	3.3	6
Minimum CTC in LPA: 3.3 LPA		**Maximum CTC in LPA: 19.00 LPA**	



Ellite: >= 15 LPA, Super Dream: >8.0 LPA, Dream: 6.0 to 8.00, LPA, Normal: < 6.0 LPA